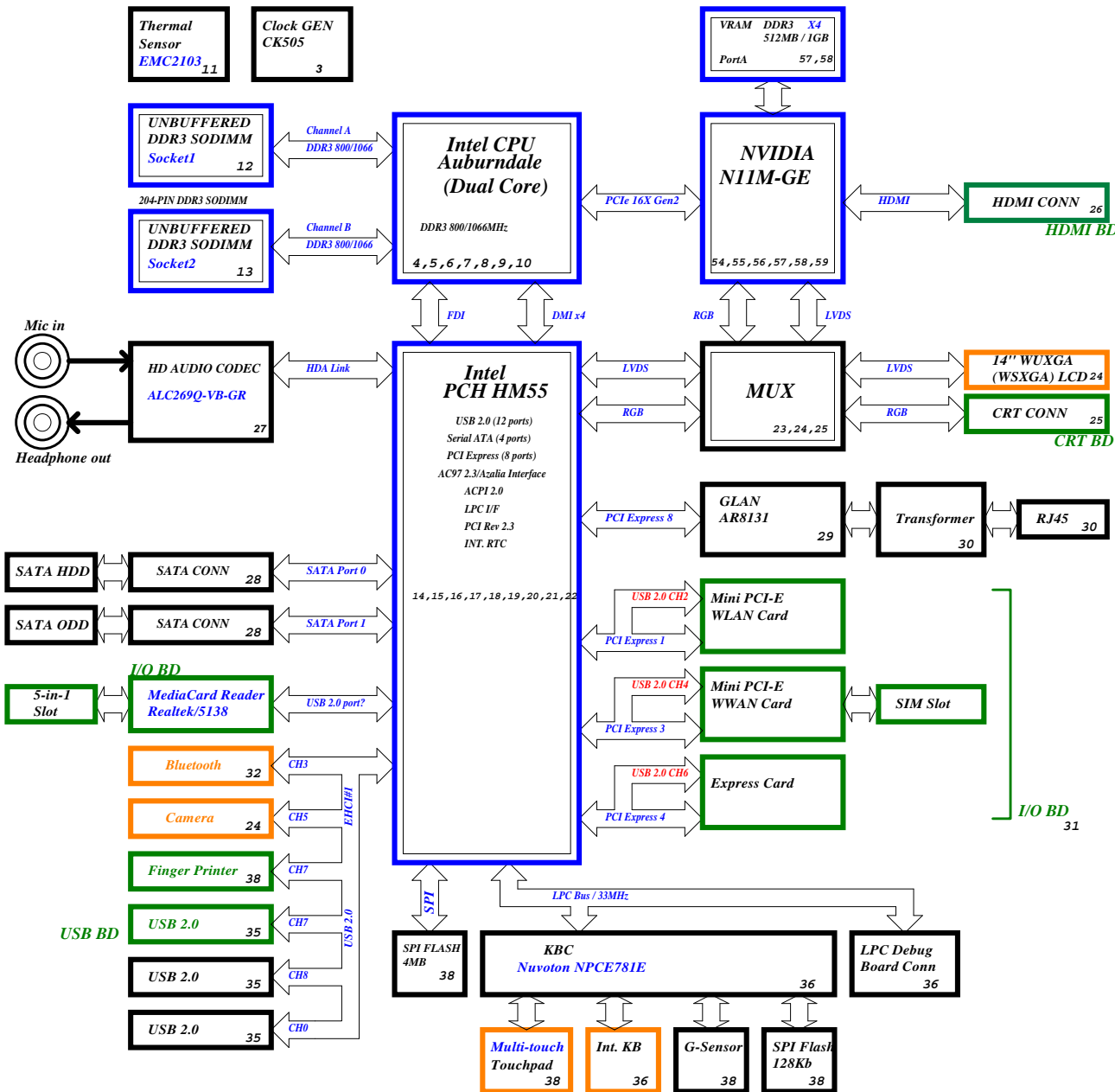


# LA46 Switchable Graphics System Schematics

Project Code: 91.4GV01.001  
PCB(Raw Card): 09911-1



- USB BD
- I/O BD
- CRT BD
- Power BD
- Finger Printer BD
- HDMI BD
- BT BD
- AV BD

PCB LAYER	
L1:	Top
L2:	GND
L3:	Signal
L4:	Signal
L5:	VCC
L6:	Signal
L7:	GND
L8:	Signal

CPU DC/DC ISL62882	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS51123	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC RT8209E	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3

SYSTEM DC/DC RT8209E	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0

SYSTEM DC/DC RT8209E	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

LDO RT9025	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

LDO RT9026	
INPUTS	OUTPUTS
1D5V_S3	0D75_S0 DDR_VREF_S3

SYSTEM DC/DC ISL62881	
INPUTS	OUTPUTS
DCBATOUT	VCC GFXCORE

SYSTEM DC/DC ISL62872	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE_S0

CHARGER BQ24745	
INPUTS	OUTPUTS
DCBATOUT	BT+

<Core Design>	
緯創資通 Wistron Corporation	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsein 321, Taiwan, R.O.C	
Title 01 Block Diagram	
Size	Document Number
Customer	LA46 MB DIS
Date: Wednesday, January 27, 2010	Sheet 1 of 58

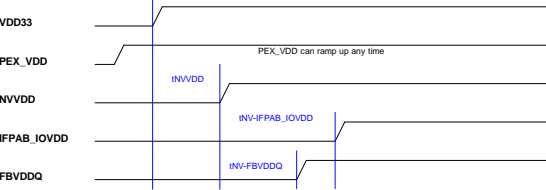
Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	Reserved - Temporarily used for early Clarkfield samples.	Clarkfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor <b>Note:</b> Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

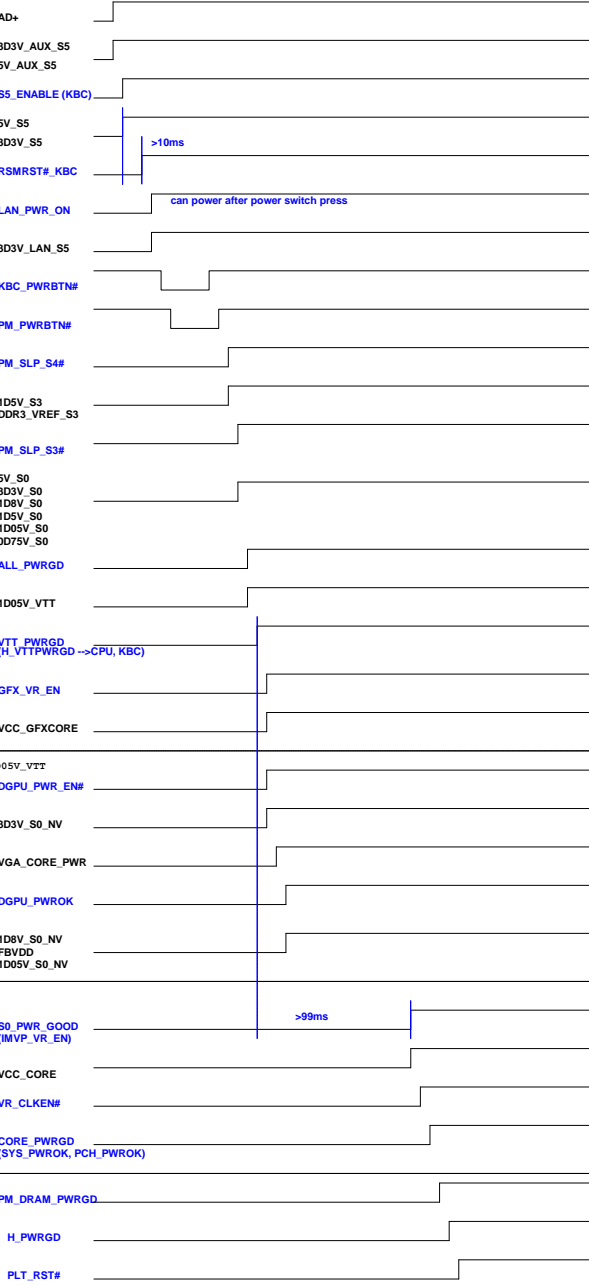
PCH Strapping

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap Mode (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled
GNT0#, GNT1#	Default (SPI): Left both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	Default - Internal pull-up. Low (0)= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	Default: Do not pull low. Disable ME in Manufacturing Mode: Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable iTPM: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0): Flash Descriptor Security will be overridden. High (1) : Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

N11M-GE Power Sequence

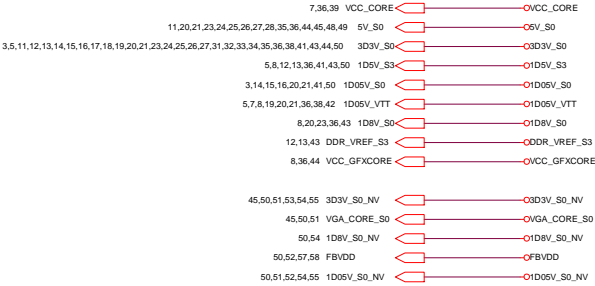


Sequence AC

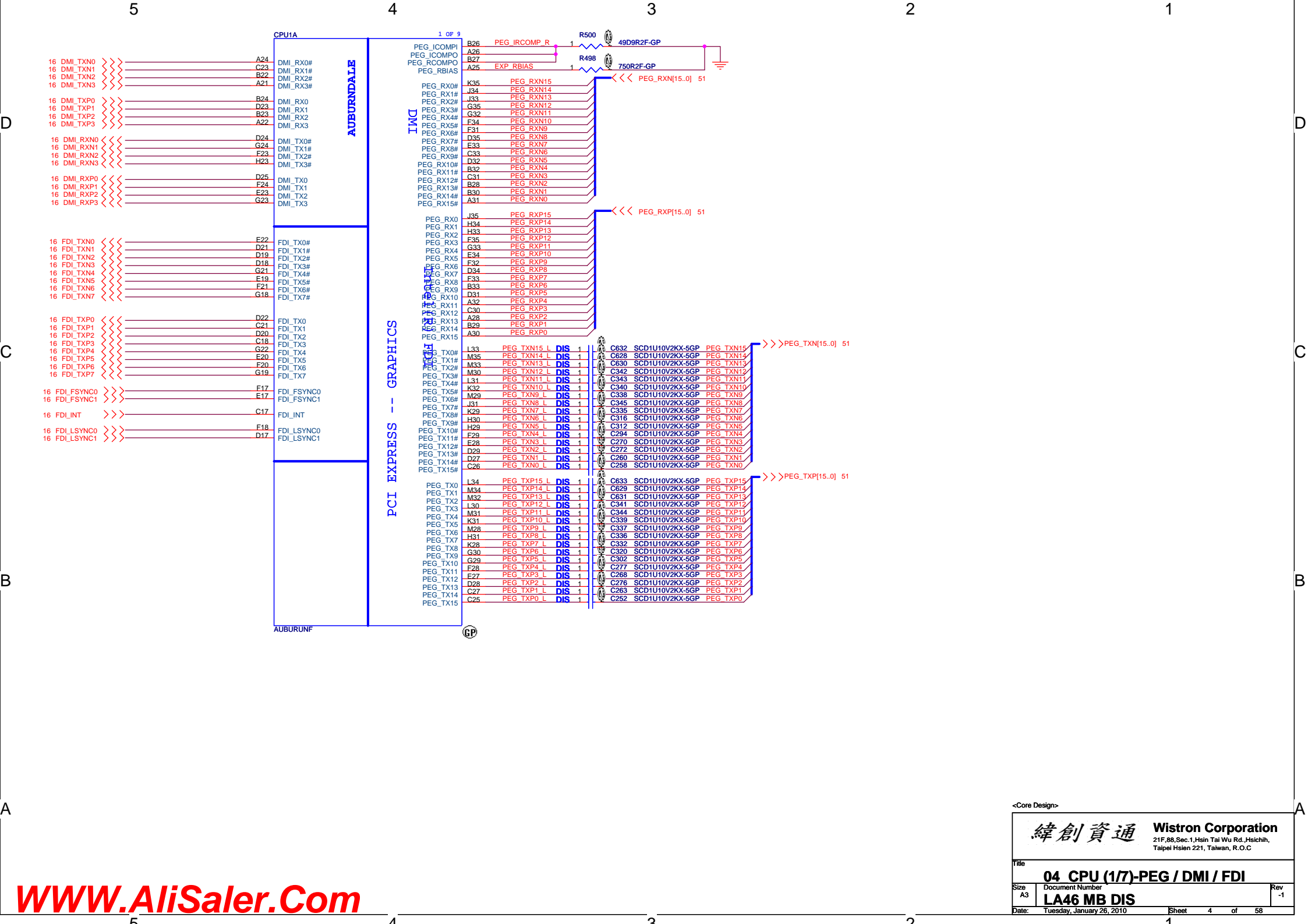


PLANAR\_ID[1..0]

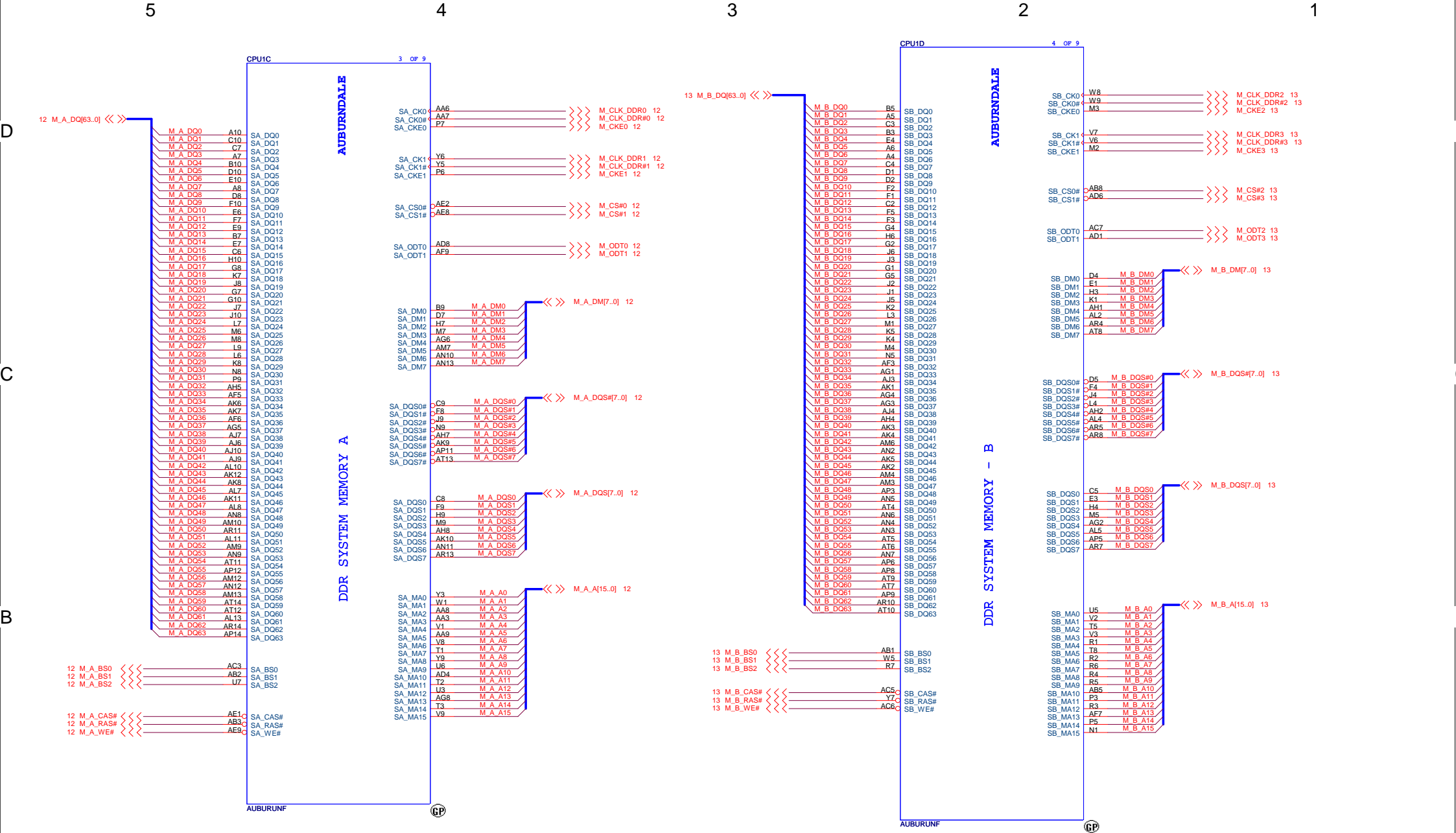
KBC GPin	31	23	Planar ID Version	Planar PCB Version
PLANAR_IDn	1	0	LA46 - SA	SA
	0	0	LA46 - SB	SB
	0	1	LA46 - SB	SC
	1	0		
	1	1		-1

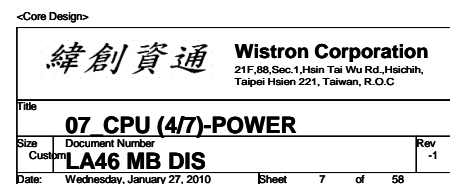
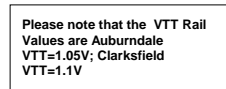
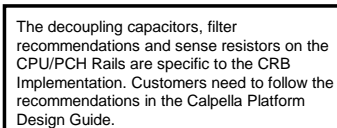
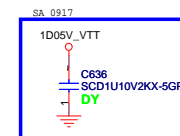
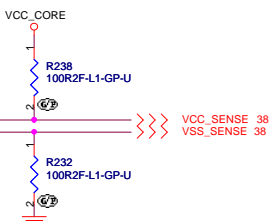
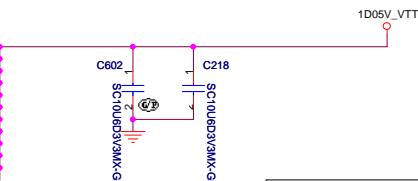
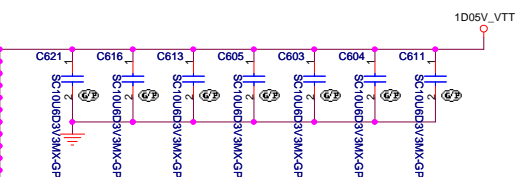
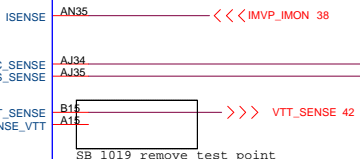
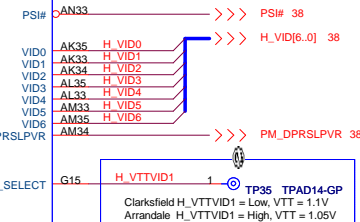
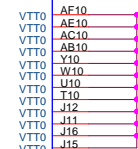


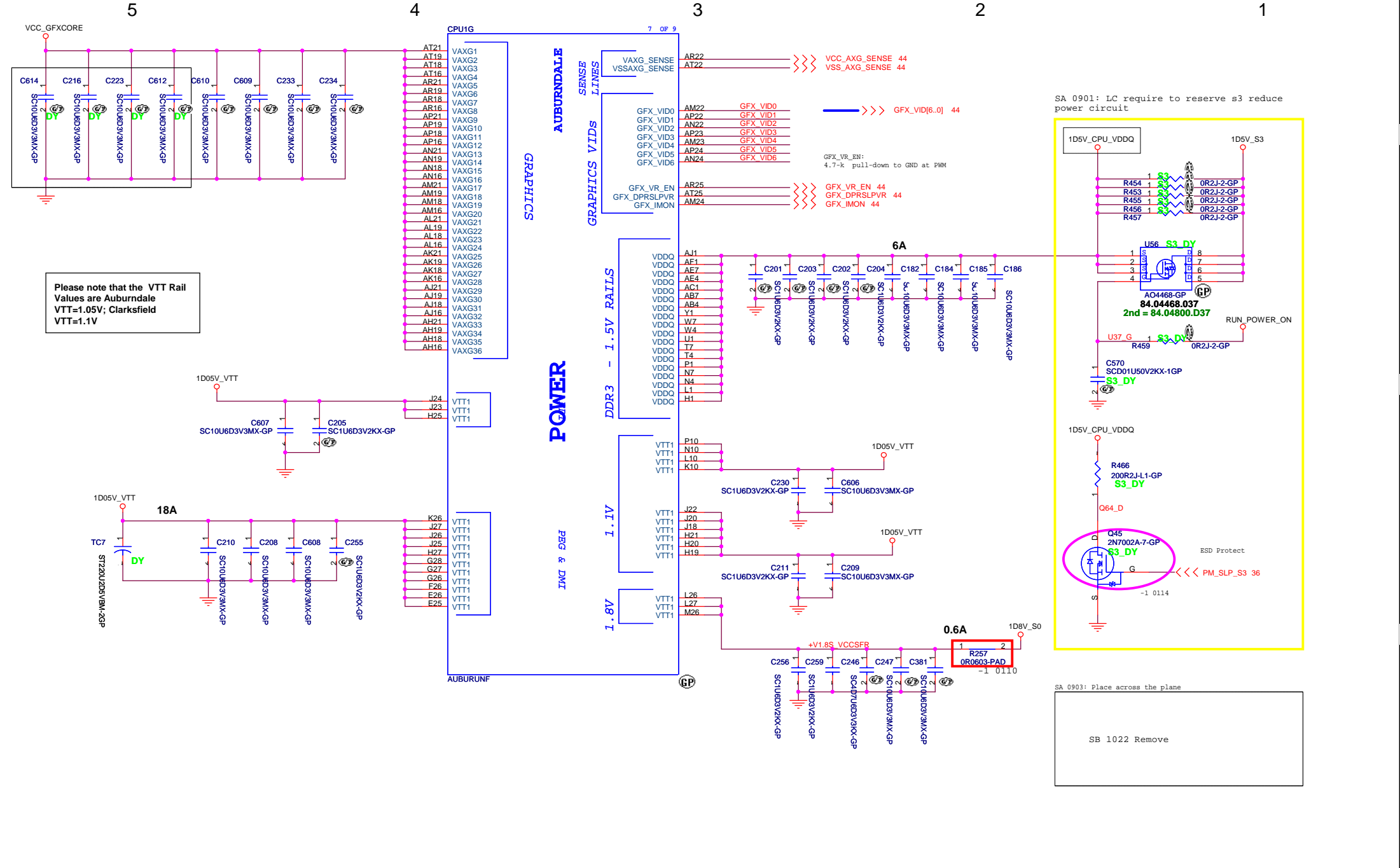




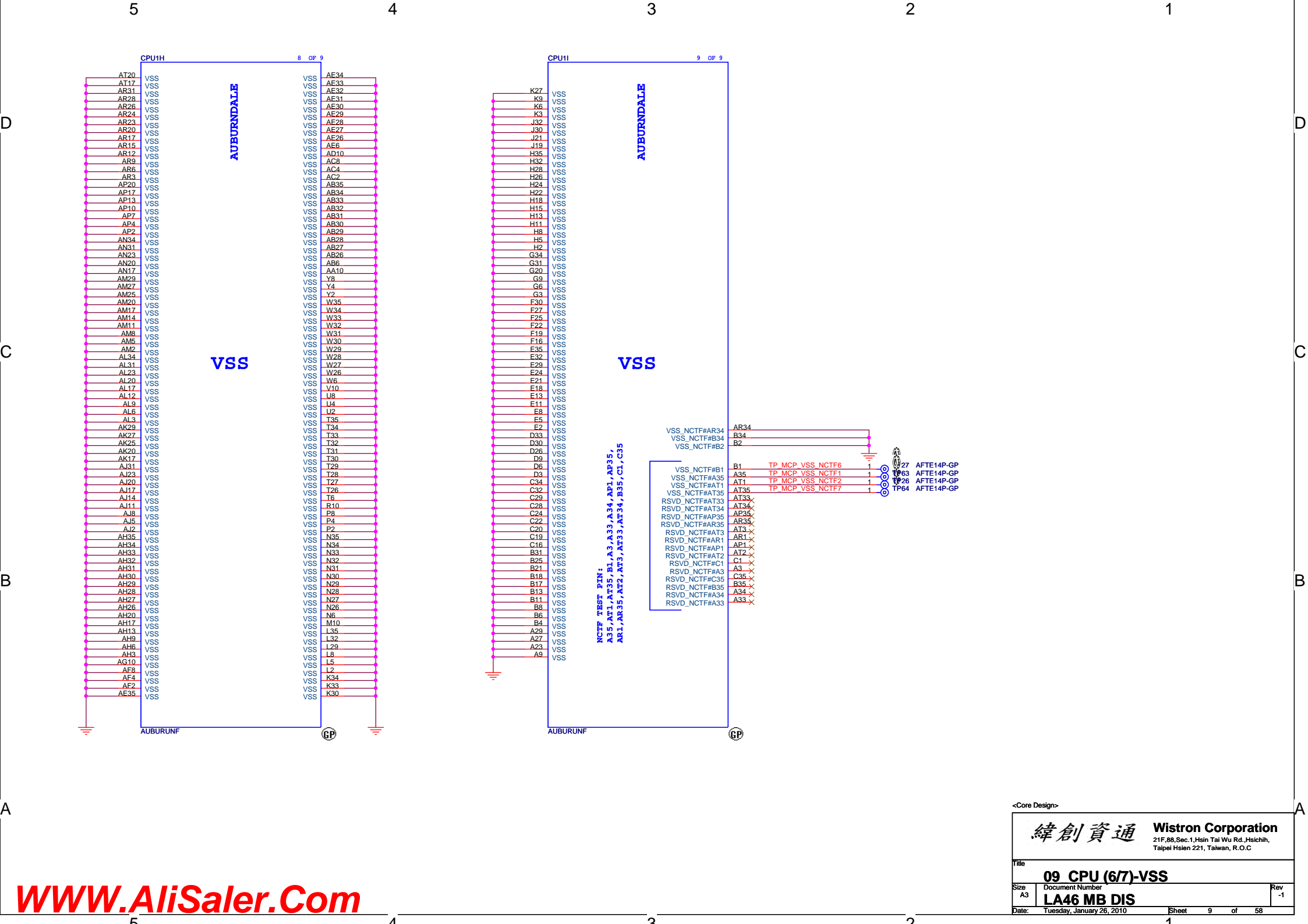


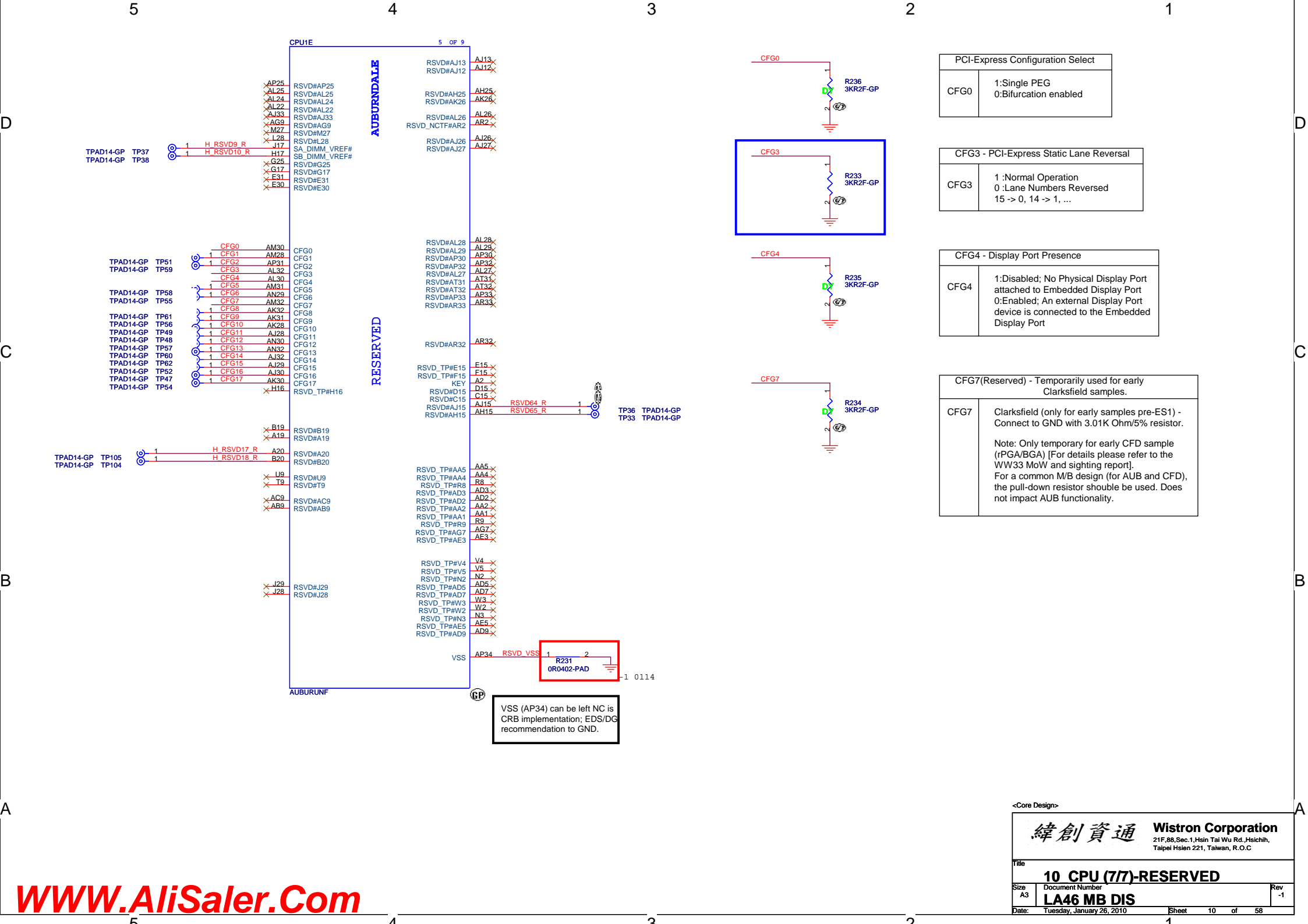


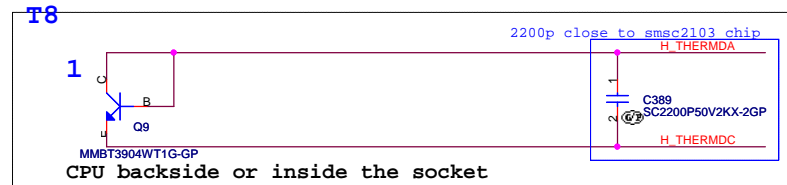
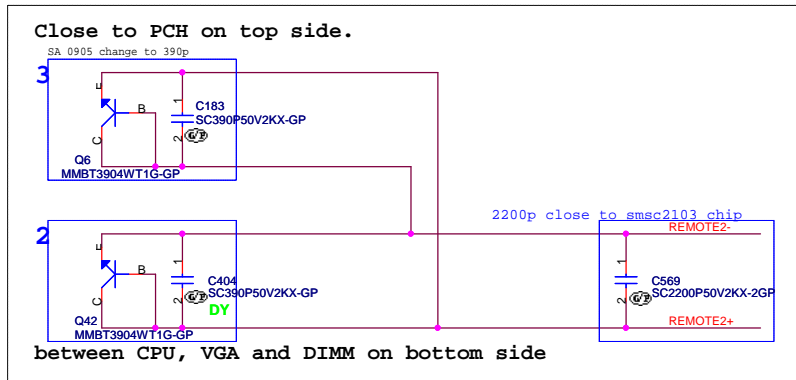




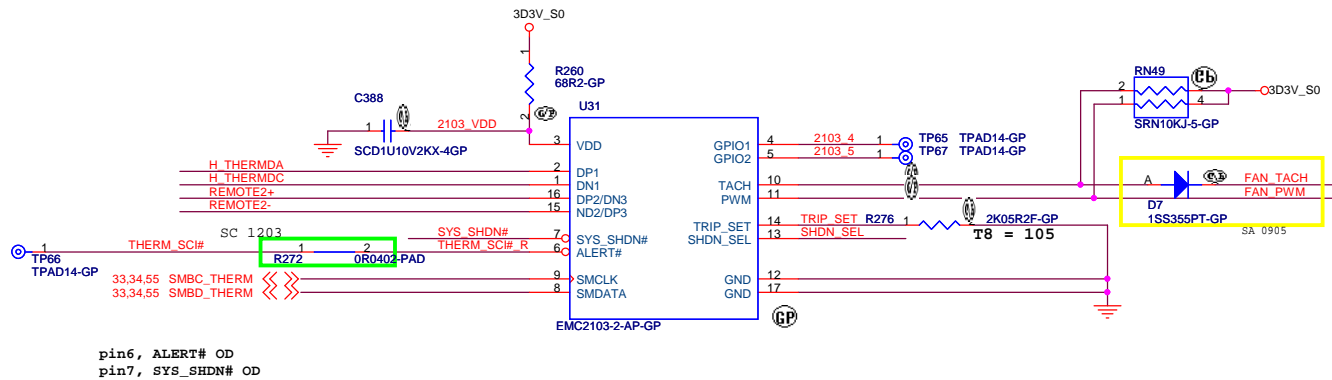
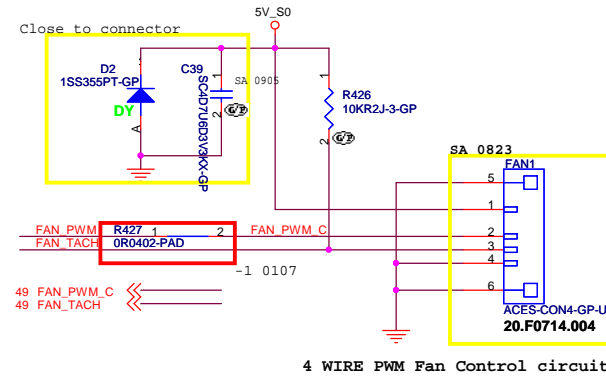
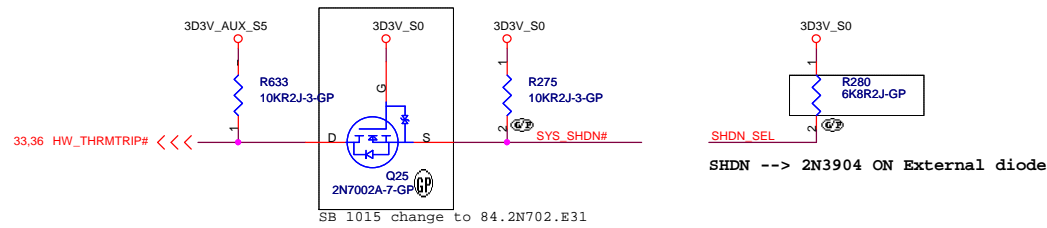








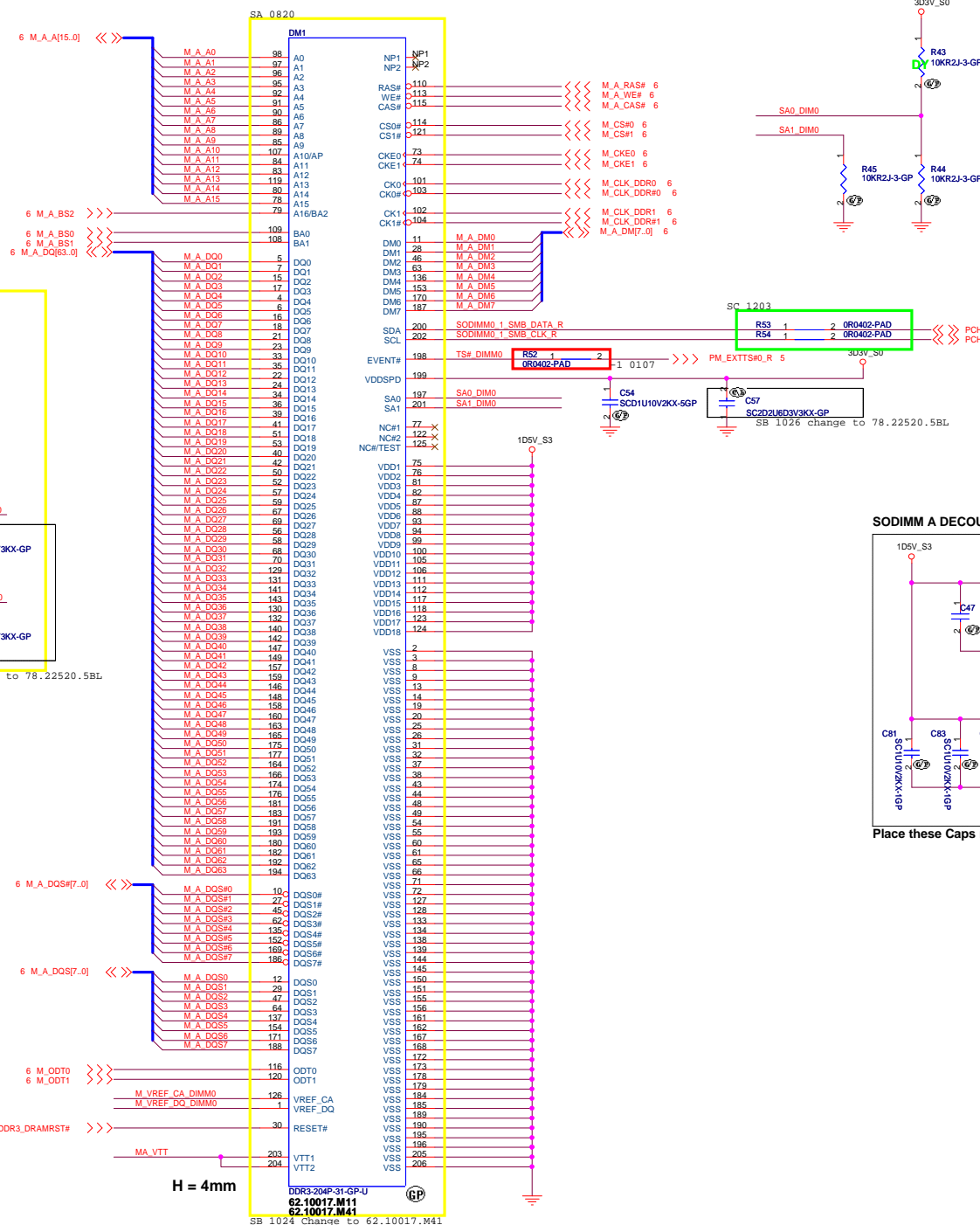
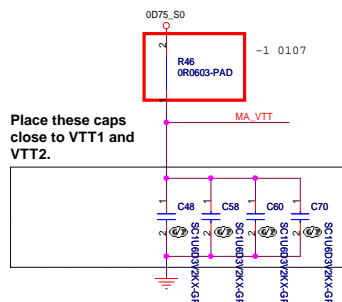
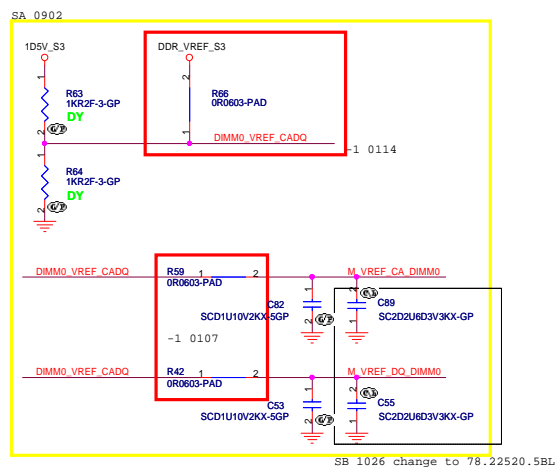
CPU TEMP:  
H\_THERMDA and H\_THERMDC routing 10mil trace width  
and spacing. Locate Capacity near Thermal diode.



<Core Design>

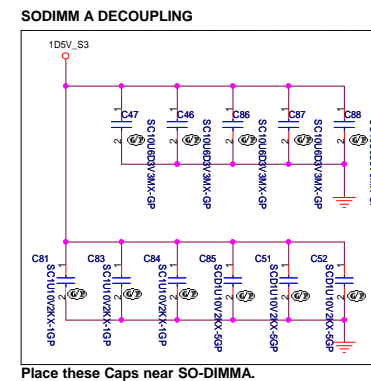
緯創資通 Wistron Corporation  
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C

Title	11 THERMAL SMSC2103		
Size	Document Number	LA46 MB DIS	
Date:	Tuesday, January 26, 2010	Sheet	11 of 58
Rev	-1		

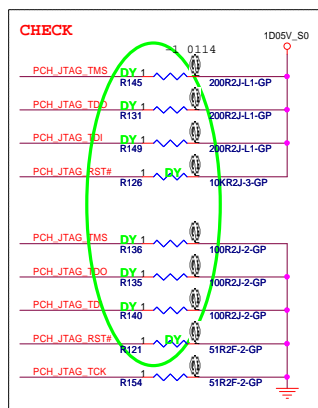
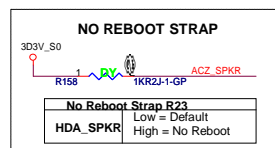
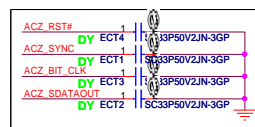
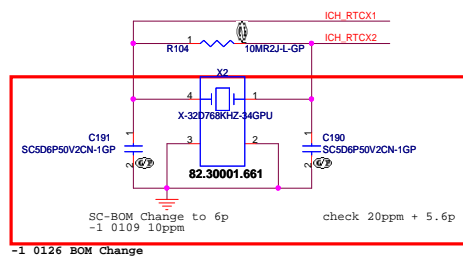


**Note:**  
If SA0\_DIM0 = 0, SA1\_DIM0 = 0  
SO-DIMMA SPD Address is 0xA0  
SO-DIMMA TS Address is 0x30

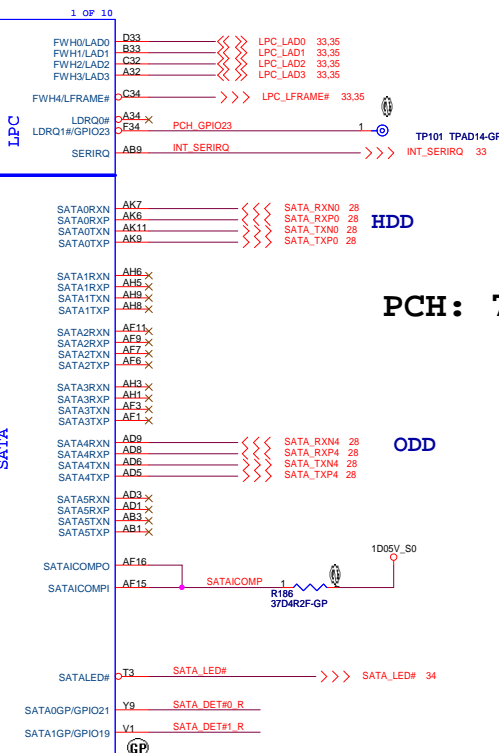
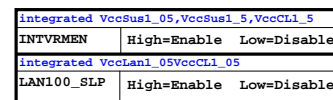
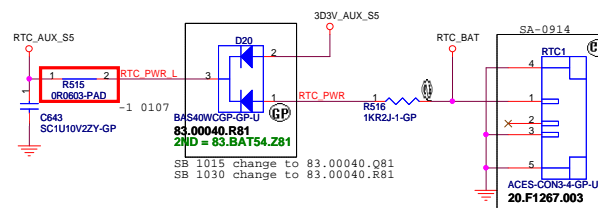
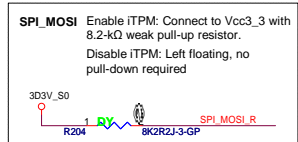
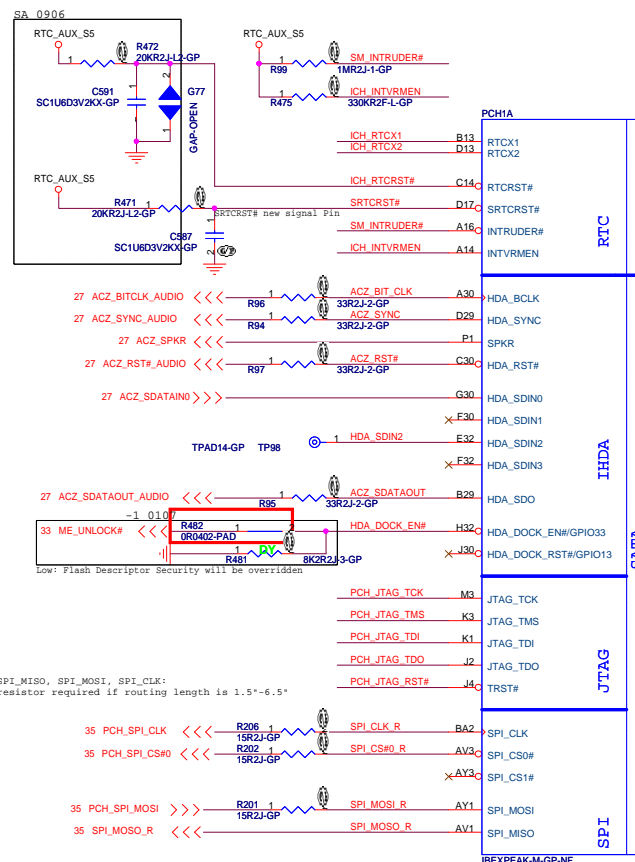
If SA0\_DIM0 = 1, SA1\_DIM0 = 0  
SO-DIMMA SPD Address is 0xA2  
SO-DIMMA TS Address is 0x32



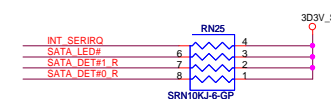




When unused all JTAG pins may be NC



PCH: 71.0IBEX.G0U

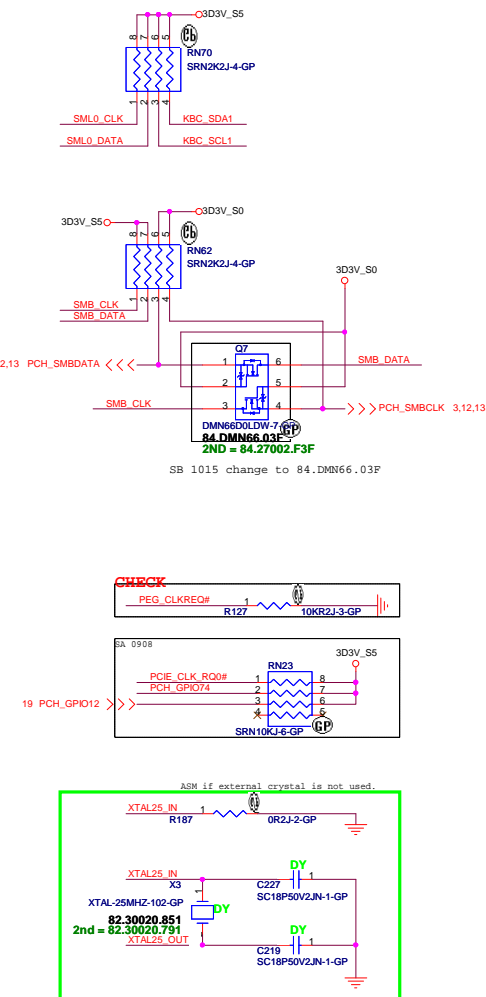


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緯創資通

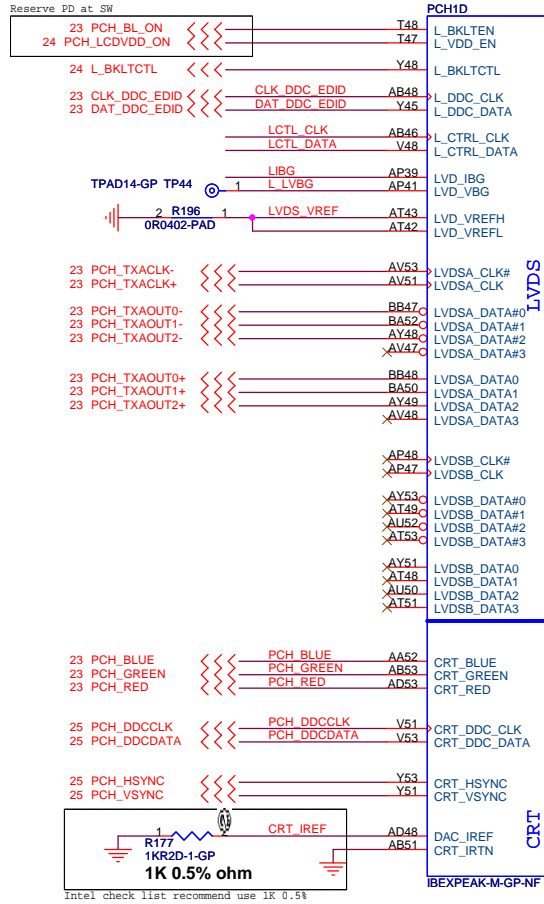
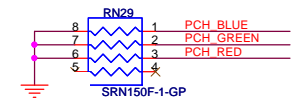
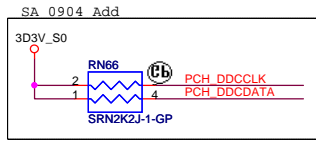
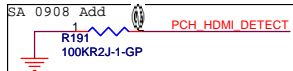
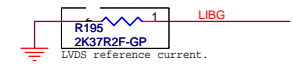
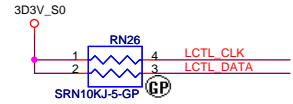
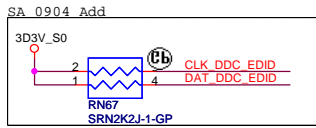
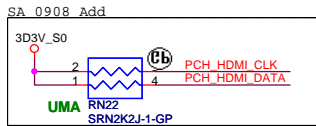
**Wistron Corporation**  
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C

Title		<b>14 PCH (1/9)-SATA/SP/LPC/HD</b>	
Size	Document Number	Rev	
Custom	<b>LA46 MB DIS</b>		
Date:	Wednesday, January 27, 2010	Sheet	14 of 58

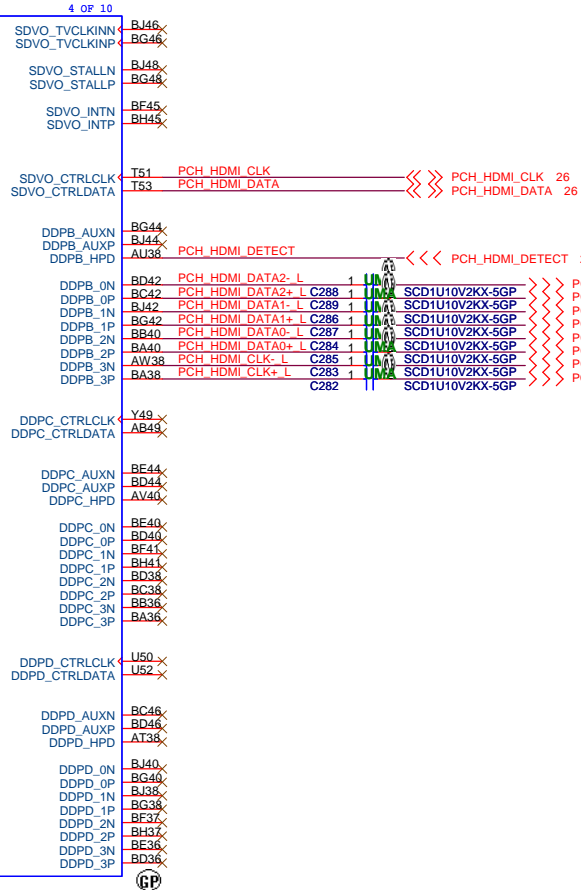






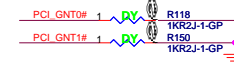
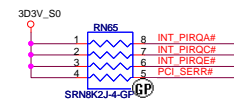
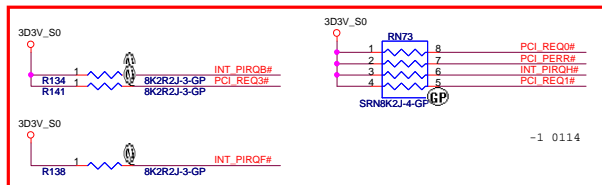
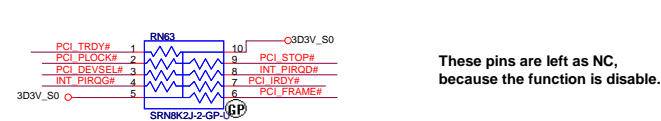


Digital Display Interface

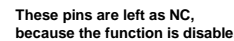
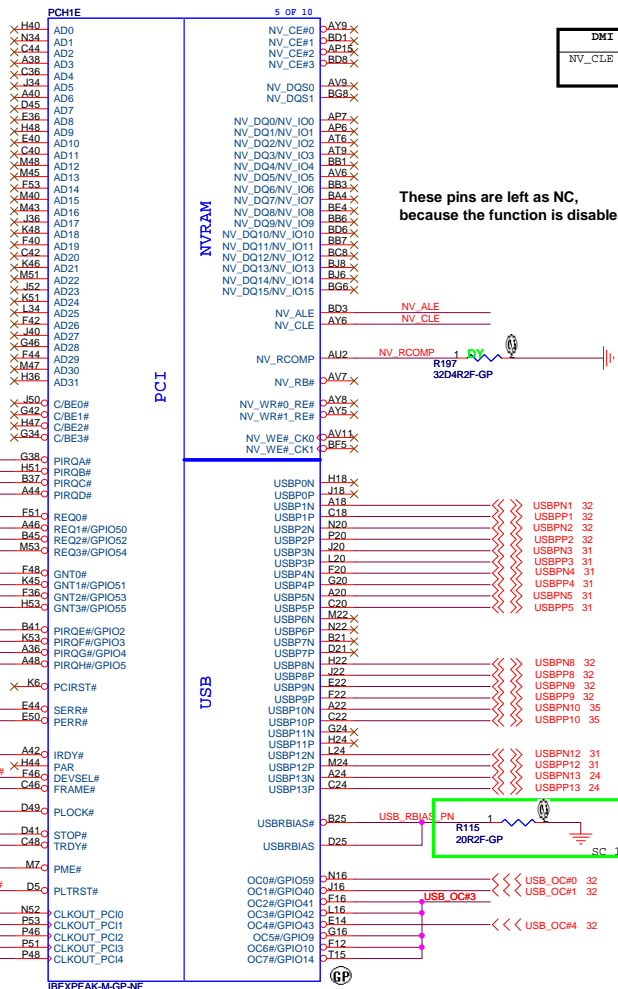
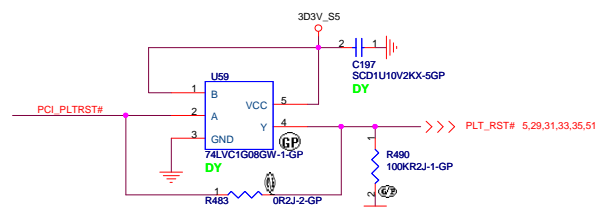
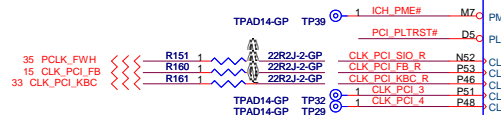


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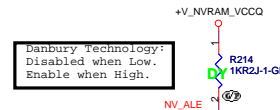
<b>緯創資通</b> Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>17 PCH (4/9)-LVDS / CRT</b>	
Size A3	Document Number <b>LA46 MB DIS</b>
Date Tuesday, January 26, 2010	Sheet 17 of 58



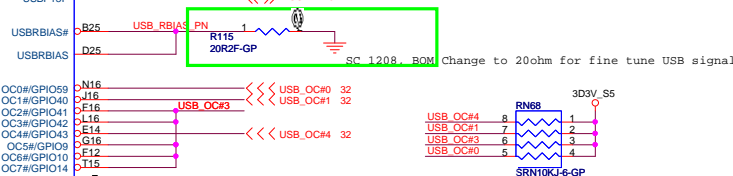
BOOT BIOS Strap		
Pci_GNT#0	Pci_GNT#1	BOOT BIOS Location
0	0	LPC(Default)
1	0	Reserved
0	1	PCI
1	1	SPI



DMI Termination Voltage	
NV_CLE	Set to Vss when low. Set to Vcc when high



Pair	Device
0	NC
1	USB3
2	USB1
3	WLAN
4	Card Reader
5	WWAN
6	Disable (HM55)
7	Disable (HM55)
8	USB2
9	Blue Tooth
10	Finger Print
11	NC
12	Express Card
13	Camera



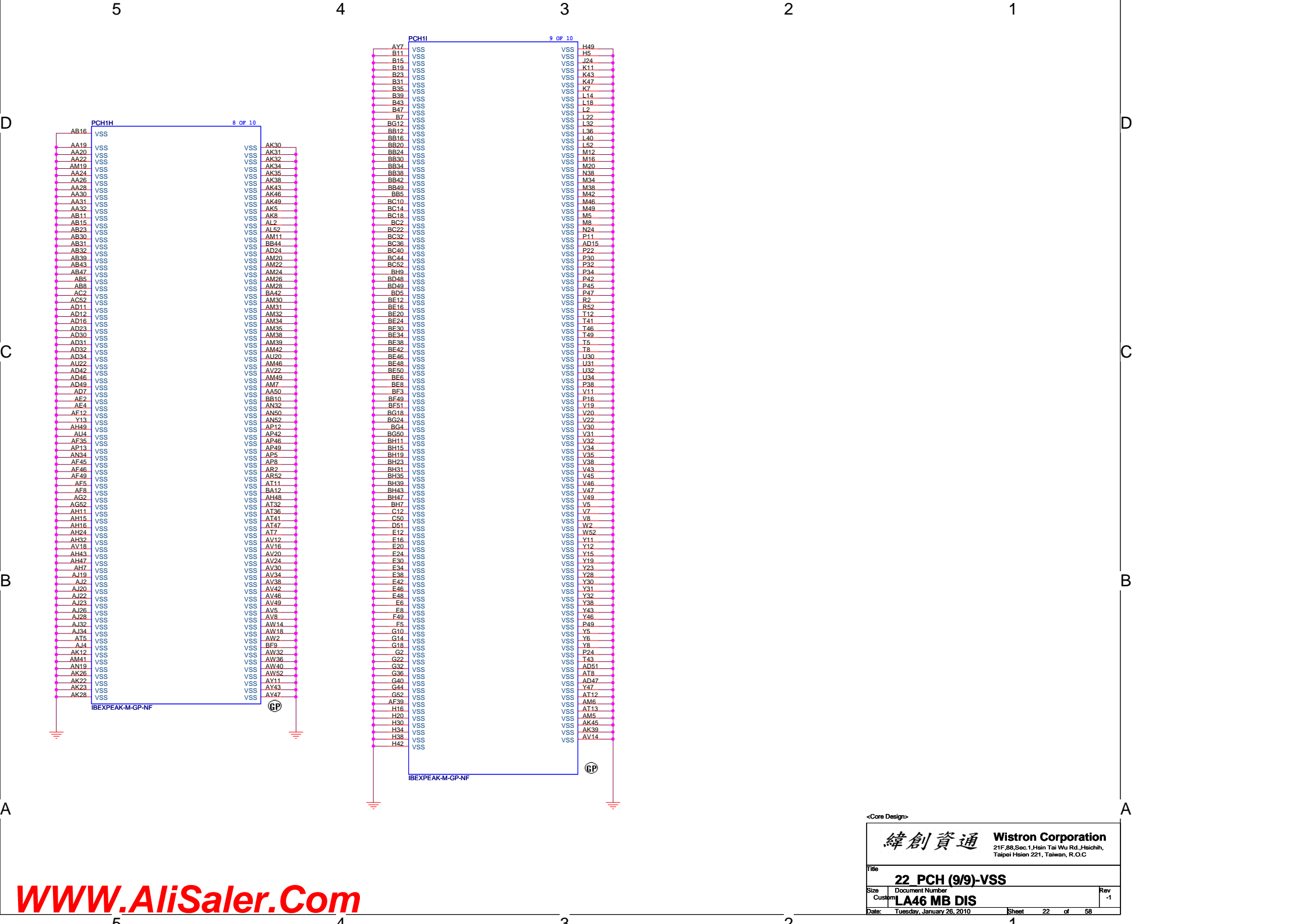
A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

OC#0	Port 0 & 1	EHCI
OC#1	Port 2 & 3	
OC#2	Port 4 & 5	
OC#3	Port 6 & 7	
OC#4	Port 8 & 9	EHCI
OC#5	Port 10 & 11	
OC#6	Port 12 & 13	
OC#7	Floater OC# (not used)	









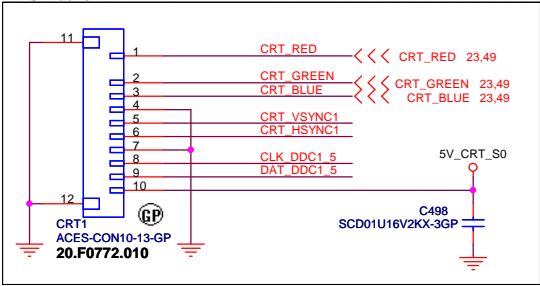




**WWW.<sup>5</sup>AliSaler.Com**



SA-0820 Move pi filter to CRT board.  
SA-0823



SB 1024 Add pin to GND (EMI)

CLK\_DDC1\_5 <<< CLK\_DDC1\_5 49  
DAT\_DDC1\_5 <<< DAT\_DDC1\_5 49

CRT\_VSYNC1 <<< CRT\_VSYNC1 49  
CRT\_HSYNC1 <<< CRT\_HSYNC1 49

### Hsync & Vsync level shift

L=>B0 -DIS  
H=>B1 -UMA

18,23,24 dGPU\_SELECT#>>>

For DIS CRT

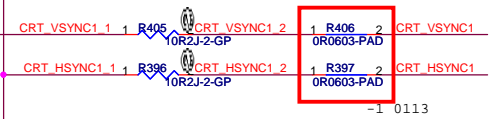
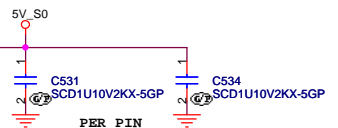
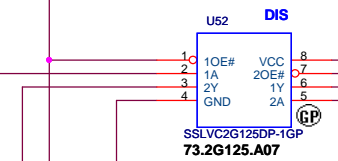
53 NV\_CRT\_HSYNC >>>

53 NV\_CRT\_VSYNC >>>

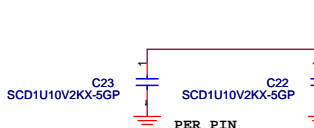
For UMA CRT

17 PCH\_HSYNC >>>

17 PCH\_VSYNC >>>

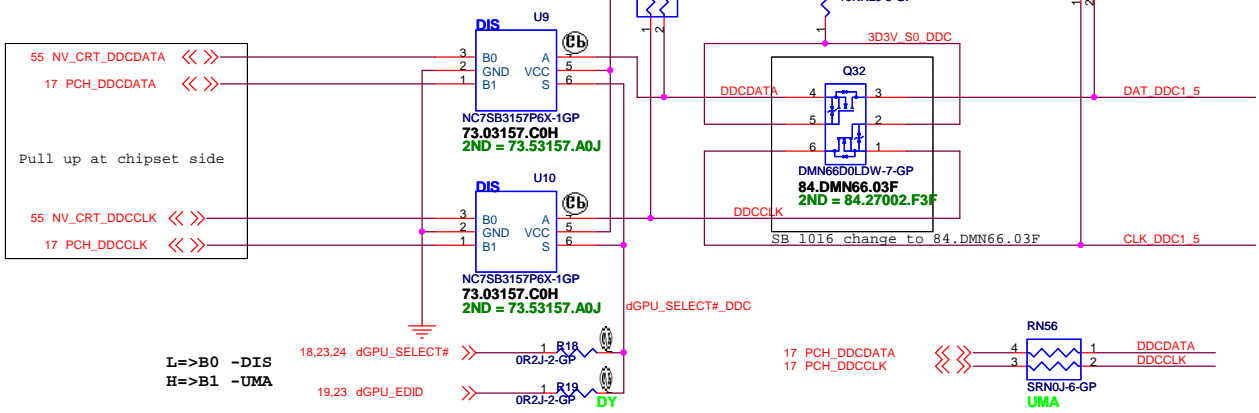


### DDC\_CLK & DATA level shift



F1 FUSE-1D1A6V-4GP-U  
69.50007.691  
2nd = 69.50007.771

D11 CH551H-30PT-GP  
83.R5003.C8F  
2nd = 83.R5003.G8H  
500mA



L=>B0 -DIS  
H=>B1 -UMA

18,23,24 dGPU\_SELECT#>>>

19,23 dGPU\_EDID >>>

17 PCH\_DDCDATA >>>

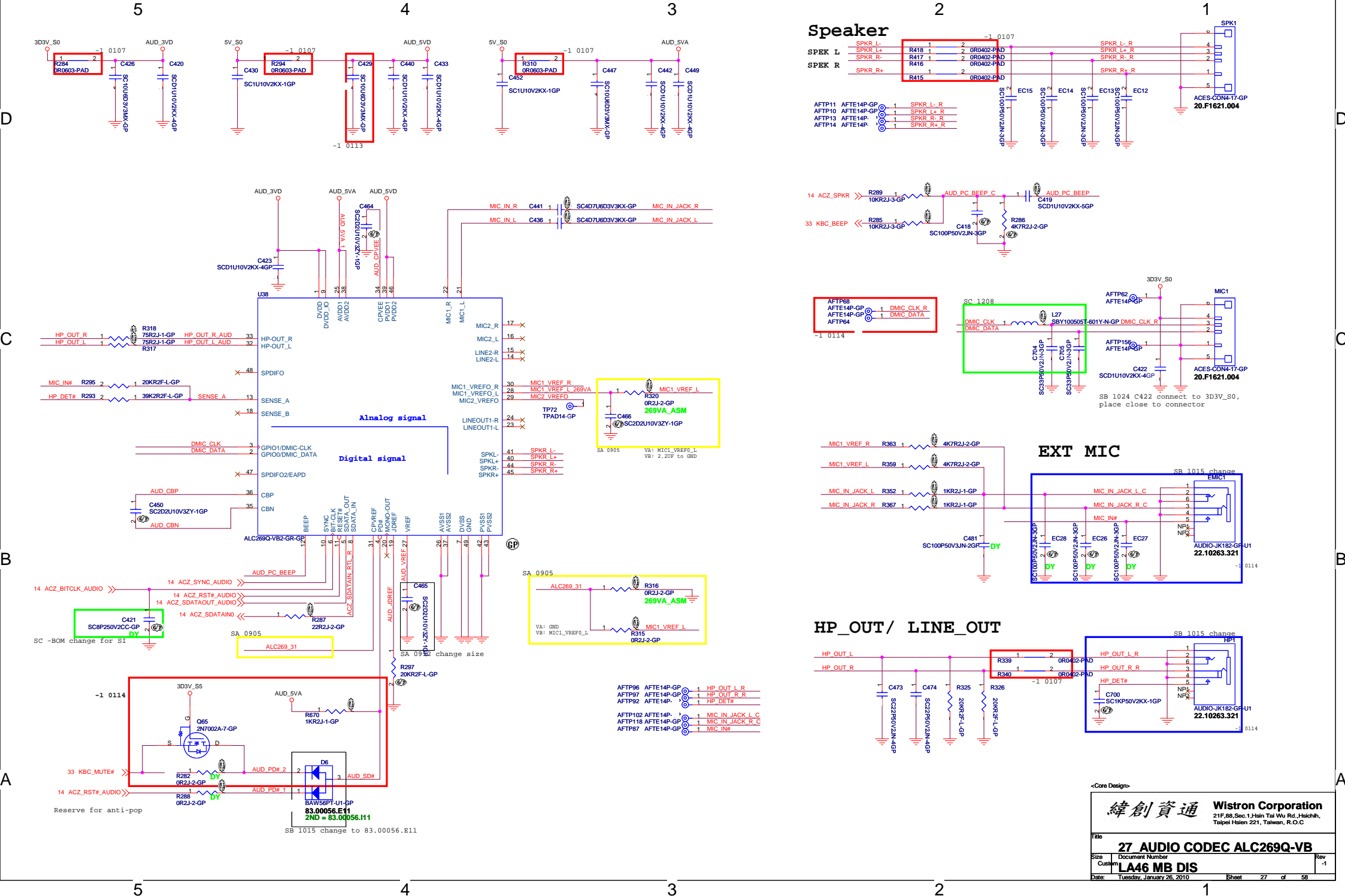
17 PCH\_DDCCLK >>>

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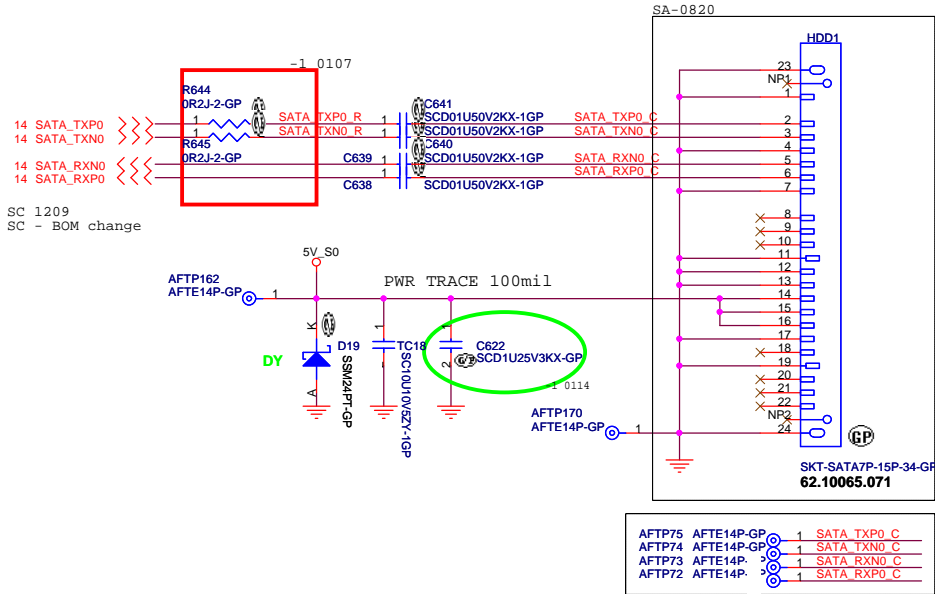
緯創資通 Wistron Corporation  
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C

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Size	A3	Document Number	LA46 MB DIS
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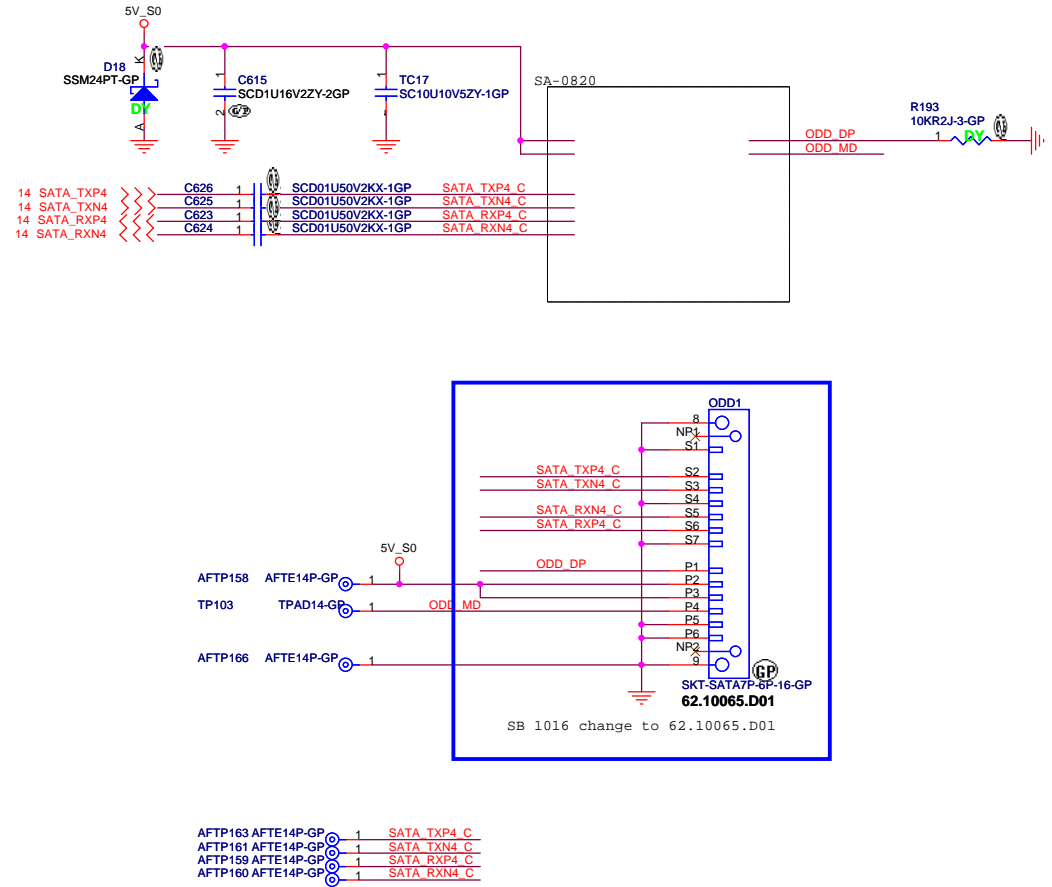




# SATA Connector



# ODD Connector



<Core Design>

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Title

28 HDD & ODD

Size

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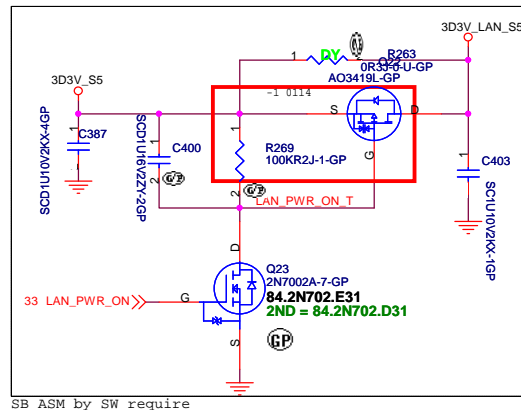
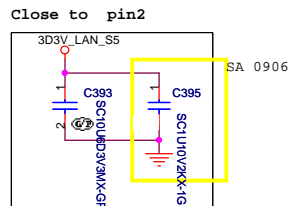
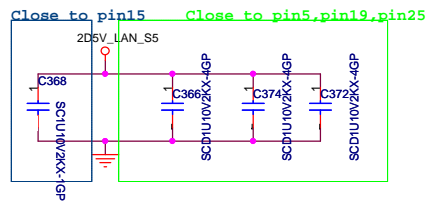
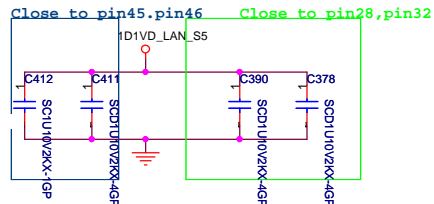
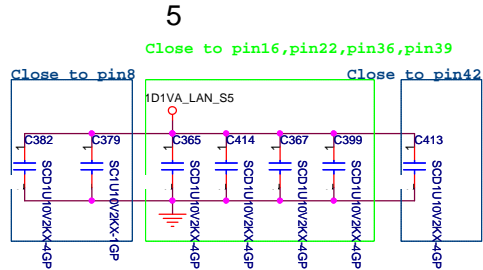
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of

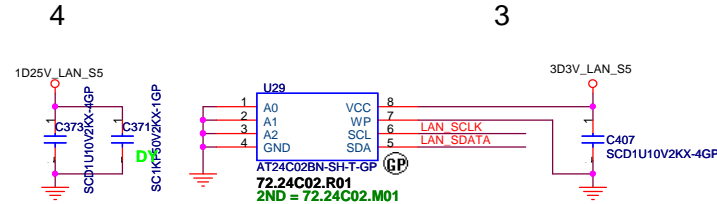
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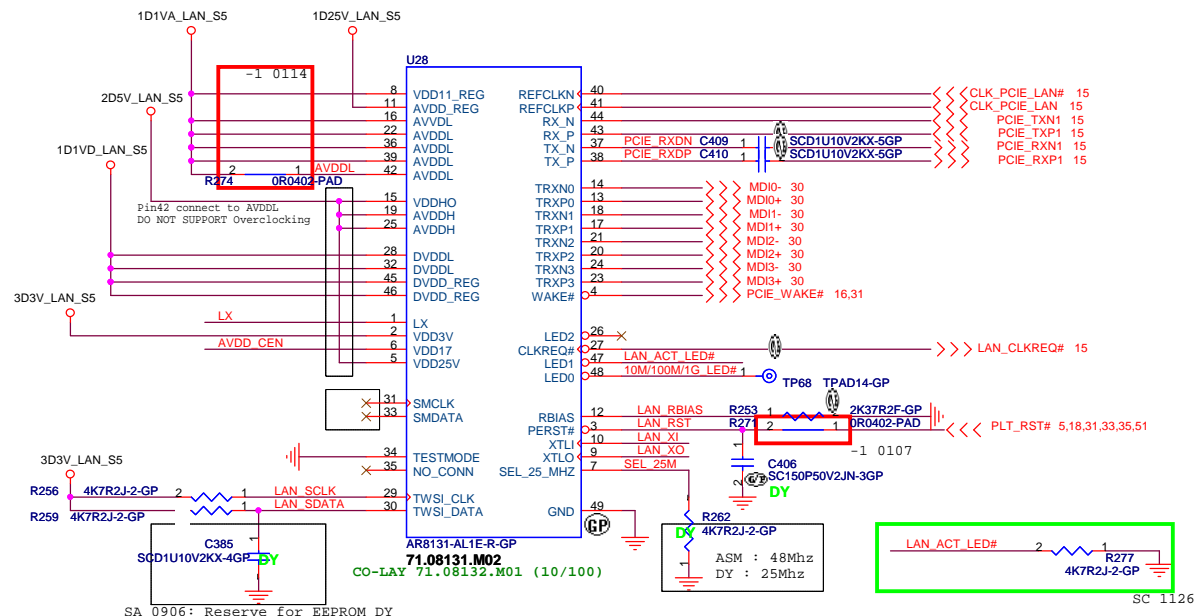
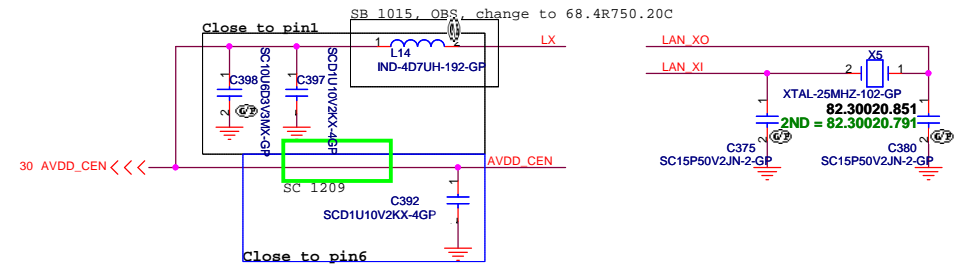
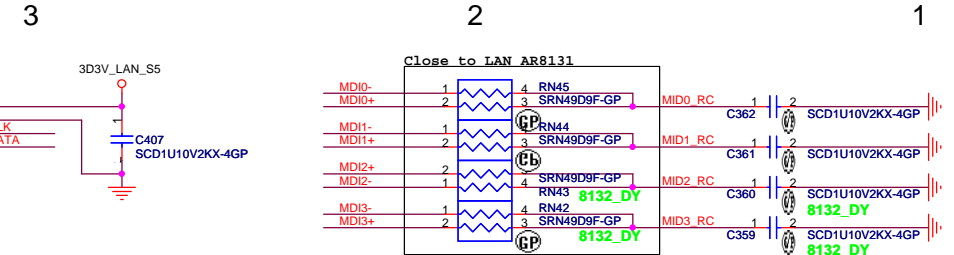
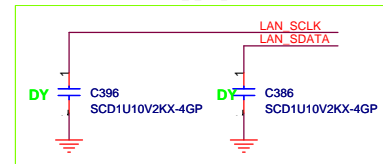
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SB ASM by SW require



for AR8131M apply in the future



**<Core Design>**

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Title			
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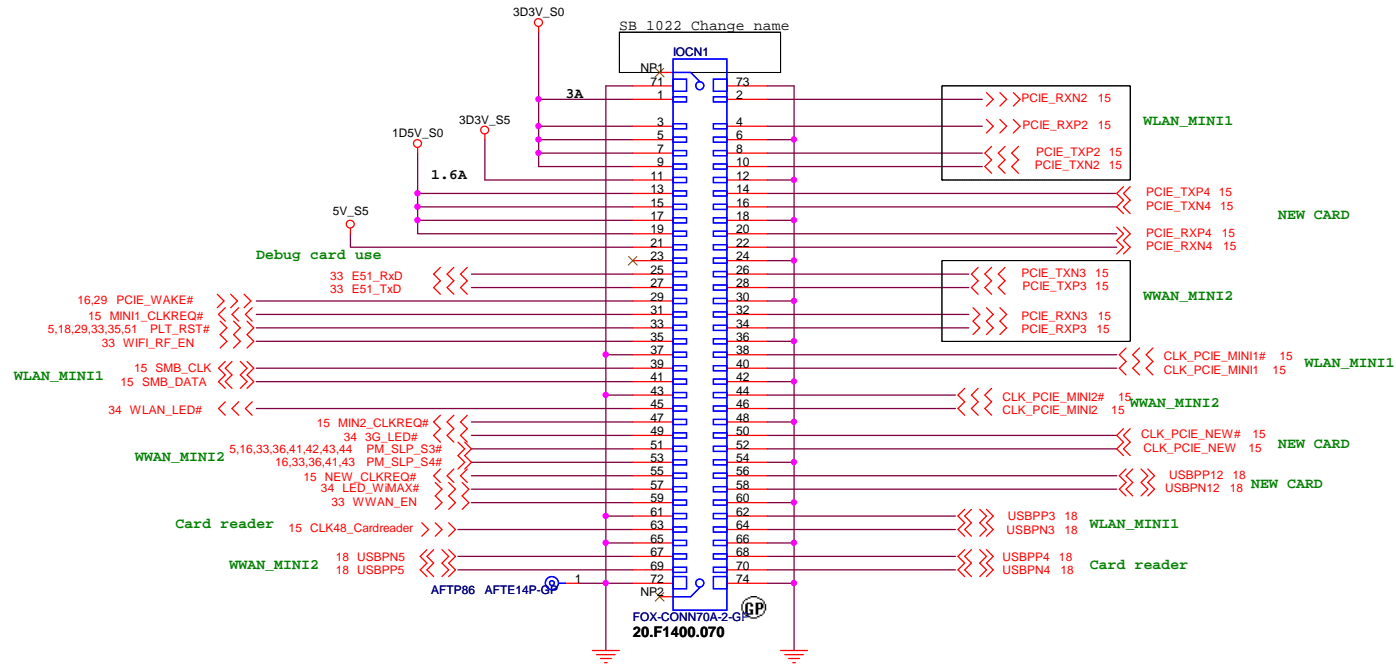
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AFTP107 AFTE14P-GP 1 3D3V\_S0  
AFTP103 AFTE14P 1 3D3V\_S5  
AFTP104 AFTE14P-GP 1 1D5V\_S0  
AFTP99 AFTE14P 1 5V\_S5

AFTP98 AFTE14P-GP 1 E51\_RxD  
AFTP93 AFTE14P-GP 1 E51\_TxD  
AFTP91 AFTE14P 1 PCIE\_WAKE#  
AFTP84 AFTE14P 1 MIN1\_CLKREQ#  
AFTP180 AFTE14P-GP 1 CLK\_PCIE\_MINI1#  
AFTP188 AFTE14P 1 CLK\_PCIE\_MINI1  
AFTP109 AFTE14P 1 PCIE\_RXN2  
AFTP108 AFTE14P 1 PCIE\_RXP2  
AFTP105 AFTE14P 1 PCIE\_TXN2  
AFTP106 AFTE14P-GP 1 PCIE\_TXP2  
AFTP185 AFTE14P 1 PLT\_RST#  
AFTP184 AFTE14P 1 WIFI\_RF\_EN  
AFTP182 AFTE14P-GP 1 SMB\_CLK  
AFTP181 AFTE14P 1 SMB\_DATA  
AFTP180 AFTE14P 1 WLAN\_LED#  
AFTP178 AFTE14P 1 MIN2\_CLKREQ#  
AFTP187 AFTE14P 1 USBPN3  
AFTP189 AFTE14P-GP 1 USBPN5  
AFTP177 AFTE14P 1 CLK\_PCIE\_MINI2#  
AFTP179 AFTE14P 1 CLK\_PCIE\_MINI2

AFTP194 AFTE14P-GP 1 USBPN4  
AFTP193 AFTE14P-GP 1 USBPN4  
AFTP176 AFTE14P-GP 1 CLK48\_Cardreader  
AFTP101 AFTE14P-GP 1 PCIE\_TXP4  
AFTP100 AFTE14P 1 PCIE\_TXN4  
AFTP95 AFTE14P 1 PCIE\_RXP4  
AFTP94 AFTE14P-GP 1 PCIE\_RXN4  
AFTP174 AFTE14P-GP 1 CLK\_PCIE\_NEW#  
AFTP173 AFTE14P 1 CLK\_PCIE\_NEW#  
AFTP80 AFTE14P 1 USBPN12  
AFTP79 AFTE14P 1 USBPN12  
AFTP81 AFTE14P-GP 1 3G\_LED#  
AFTP78 AFTE14P 1 PM\_SLP\_S3#  
AFTP82 AFTE14P 1 PM\_SLP\_S4#  
AFTP83 AFTE14P 1 NEW\_CLKREQ#  
AFTP89 AFTE14P 1 PCIE\_TXN3  
AFTP88 AFTE14P-GP 1 PCIE\_TXP3  
AFTP90 AFTE14P 1 PCIE\_RXN3  
AFTP85 AFTE14P 1 PCIE\_RXP3  
AFTP192 AFTE14P 1 USBPN5  
AFTP191 AFTE14P 1 USBPN5  
AFTP177 AFTE14P-GP 1 LED\_WMAX#  
AFTP76 AFTE14P 1 WWAN\_EN

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C

Title

31 IO CONN

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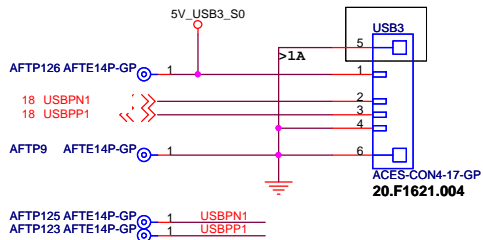
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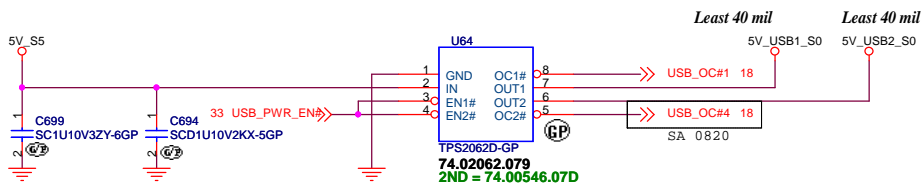
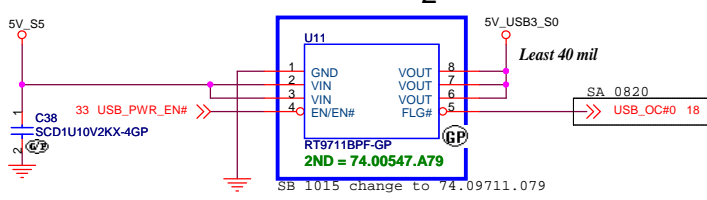
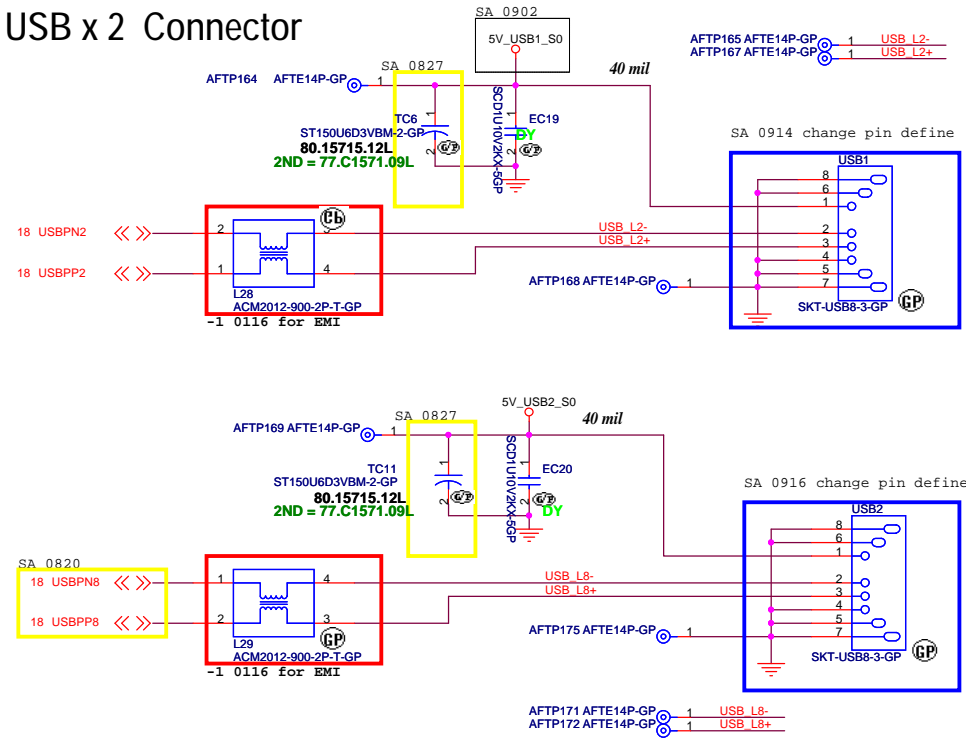
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USB3

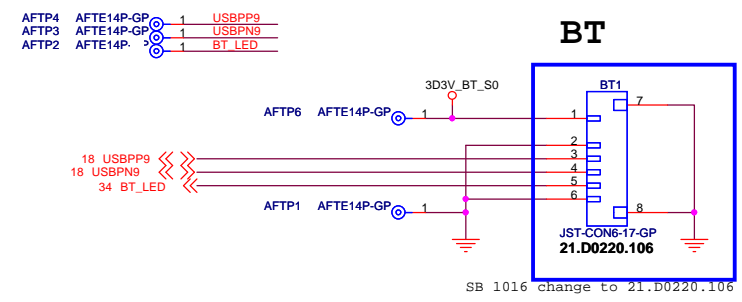
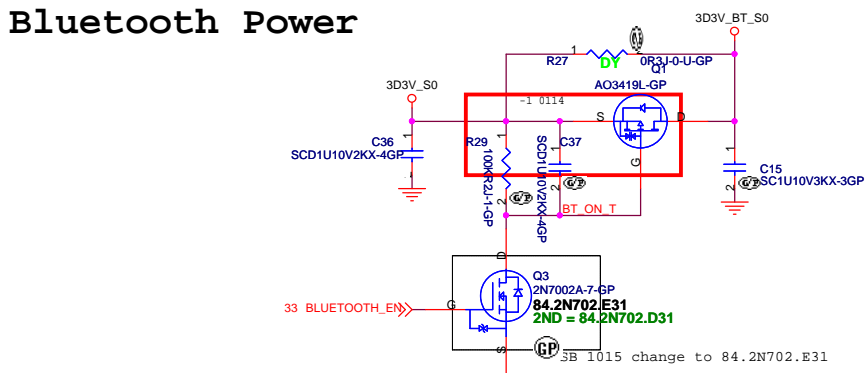
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USB x 2 Connector



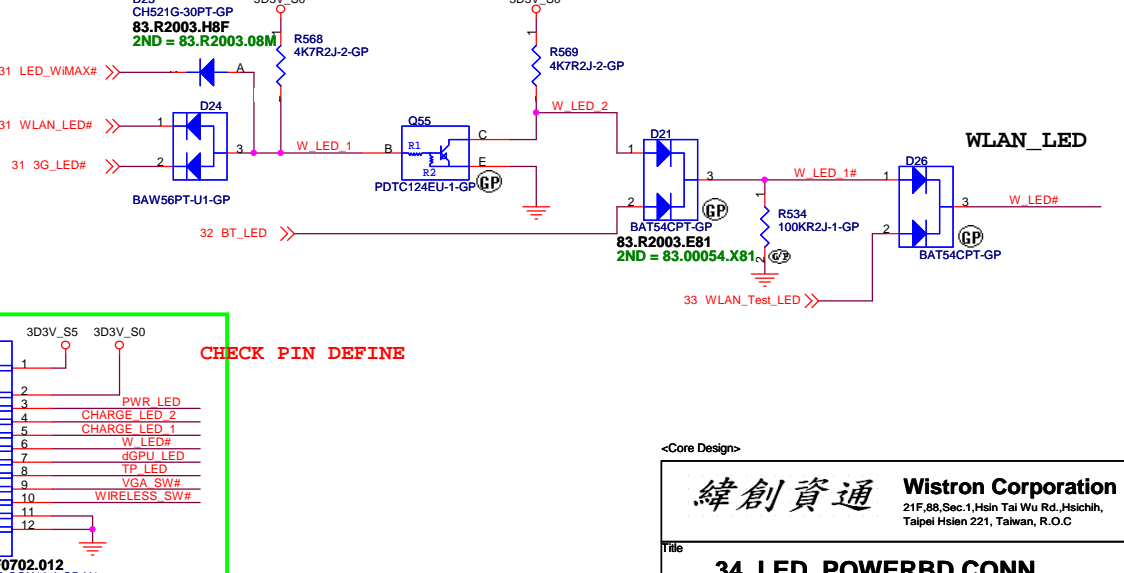
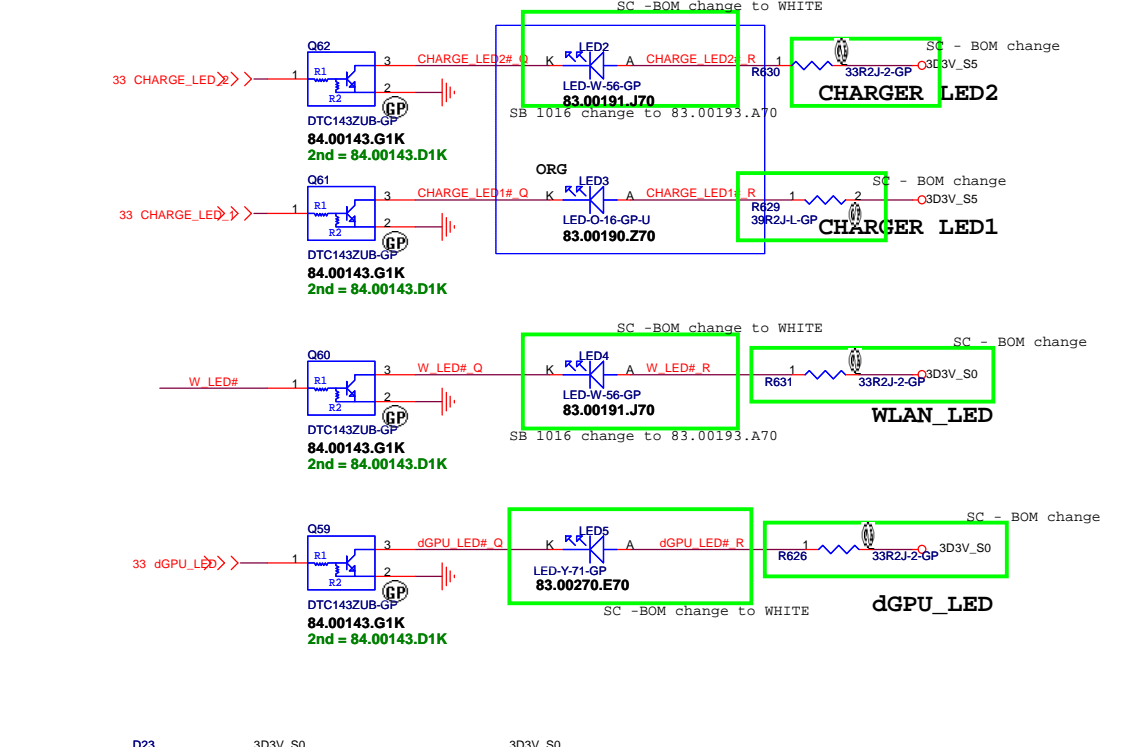
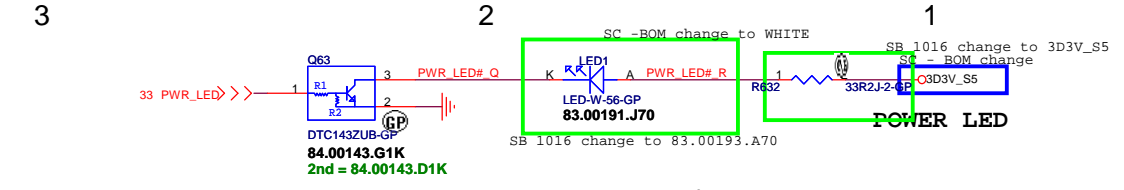
Bluetooth Power



Pin	Pin Name
1	V3V3
2	GND
3	USB D+
4	USB D-
5	LINK_IND







[illegible]

**TOUCH PAD**

5V\_S0

RN19  
SRN10KJ-5-GP

SA 0914

EC10  
SCU1010ZK4-4P

EC7  
SCU1010ZK4-4P

5V\_S0

33 TPCLK  
33 TPDATA

TPCLK  
TPDATA

SB 1015 Swap data and clk

RN21  
SRN33J-5-GP-U

1  
2

4  
3

TP CLK  
TP DATA

TP L  
TP R

SA 0904

TPAD1

1 0111

0  
6  
5  
4  
3  
2  
1  
7

ACES-CON6-13-GP

20.K0322.006

SB 1016 change to 20.K0322.006

[illegible]

# SC 1203

## GOLDEN FINGER FOR DEBUG BOARD

SB 1202

The diagram illustrates the pin connections for the Golden Finger (SB 1202) to the AFTE14P-GP connector. The connections are as follows:

- AFTE14P-GP Pin 1:** Connected to 3DVS\_S0.
- AFTE14P-GP Pin 120:** Connected to AFTE14P-GP Pin 120.
- AFTE14P-GP Pin 112:** Connected to AFTE14P-GP Pin 112.
- AFTE14P-GP Pin 116:** Connected to AFTE14P-GP Pin 116.
- AFTE14P-GP Pin 111:** Connected to AFTE14P-GP Pin 111.
- AFTE14P-GP Pin 110:** Connected to AFTE14P-GP Pin 110.
- AFTE14P-GP Pin 117:** Connected to AFTE14P-GP Pin 117.
- AFTE14P-GP Pin 114:** Connected to AFTE14P-GP Pin 114.
- AFTE14P-GP Pin 115:** Connected to AFTE14P-GP Pin 115.
- AFTE14P-GP Pin 113:** Connected to AFTE14P-GP Pin 113.

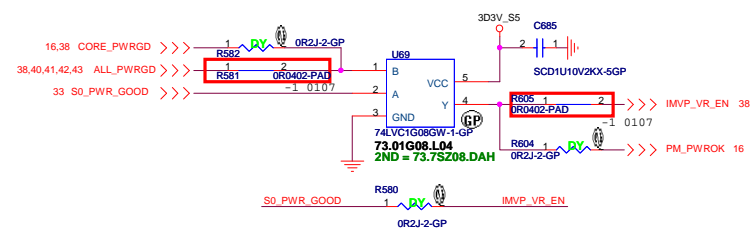
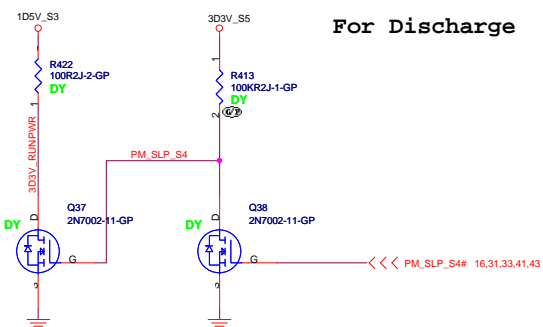
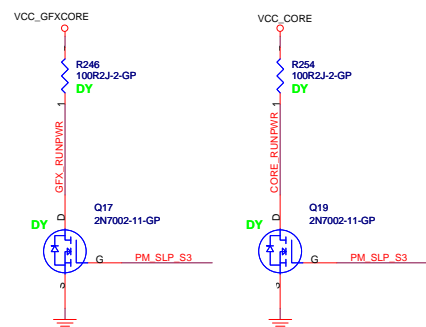
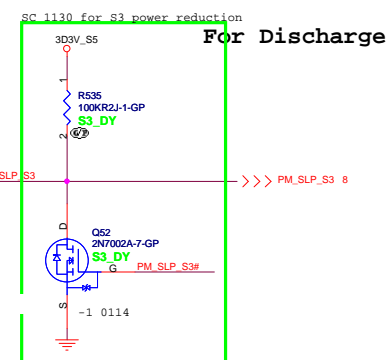
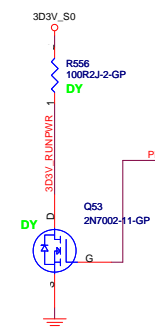
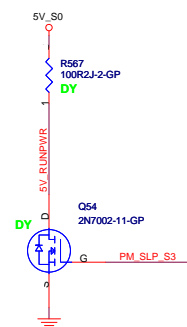
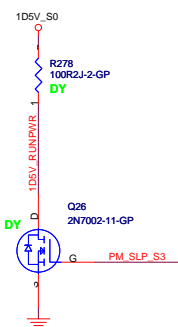
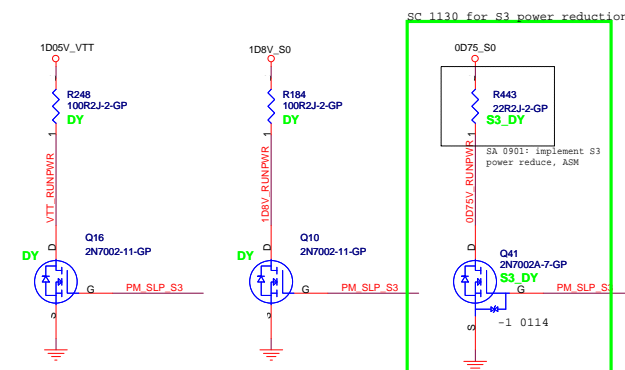
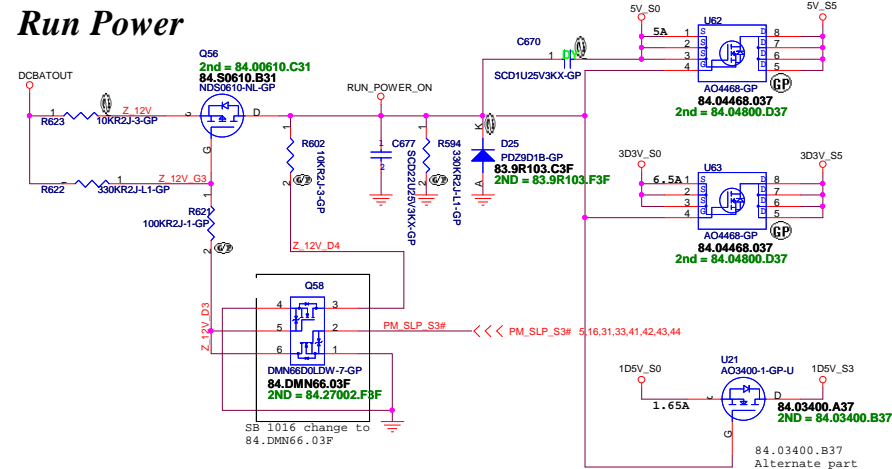
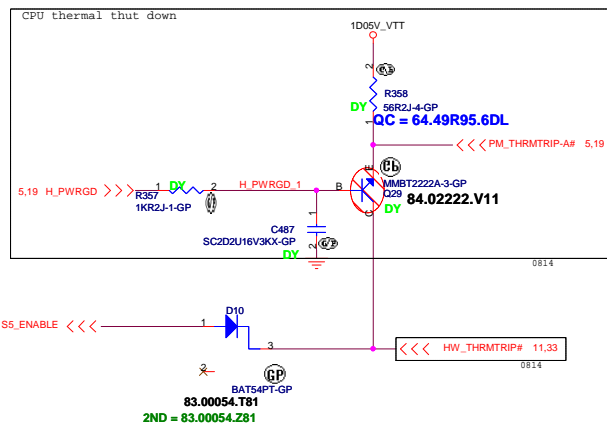
The signals connected to the Golden Finger are:

- 14.33 LPC\_LAD0
- 14.33 LPC\_LAD1
- 14.33 LPC\_LAD2
- 14.33 LPC\_LAD3
- 14.33 LPC\_LFRAME#
- 5.18,29,31,33,51 PLT\_RST#
- 18 PCLK\_FWH

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Title	35 BIOS & TP & G-Sensor & FP
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&lt;Core Design&gt;

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Title	<b>36_Run PWR</b>
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Size	Document Number
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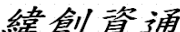
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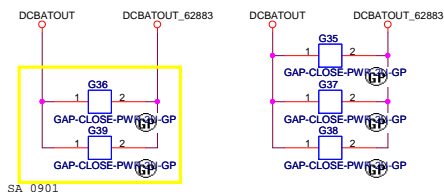
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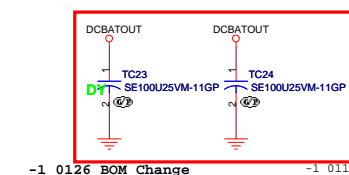
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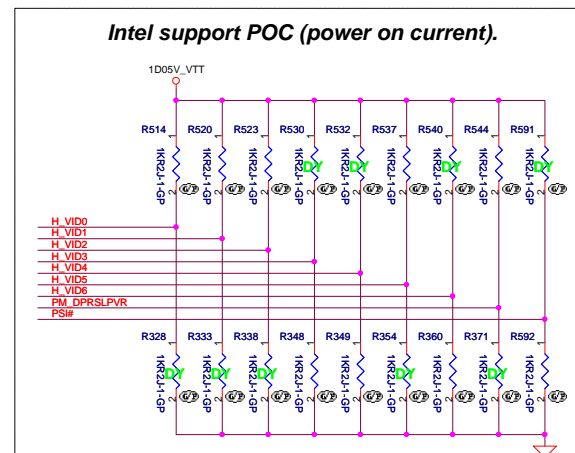
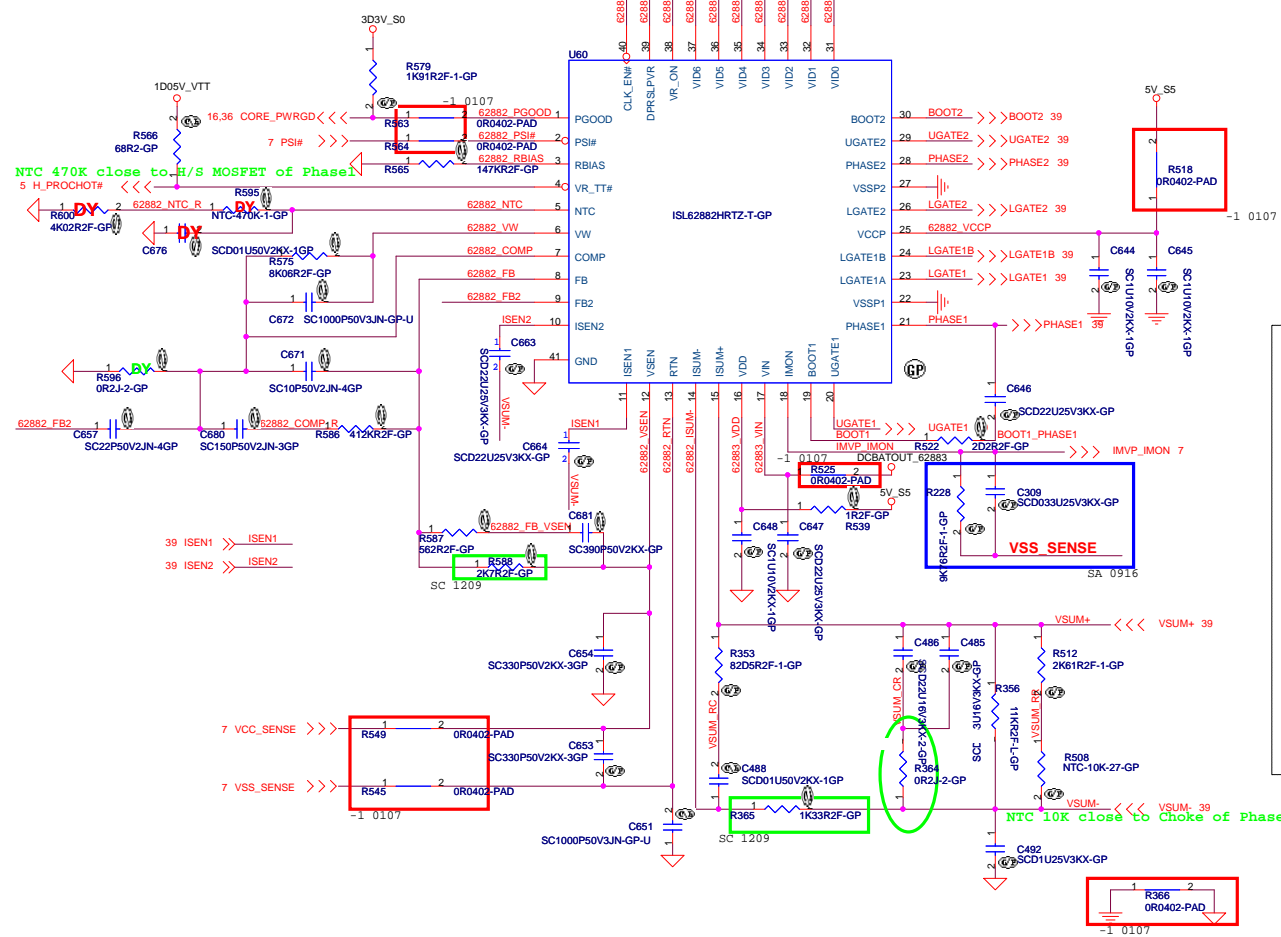
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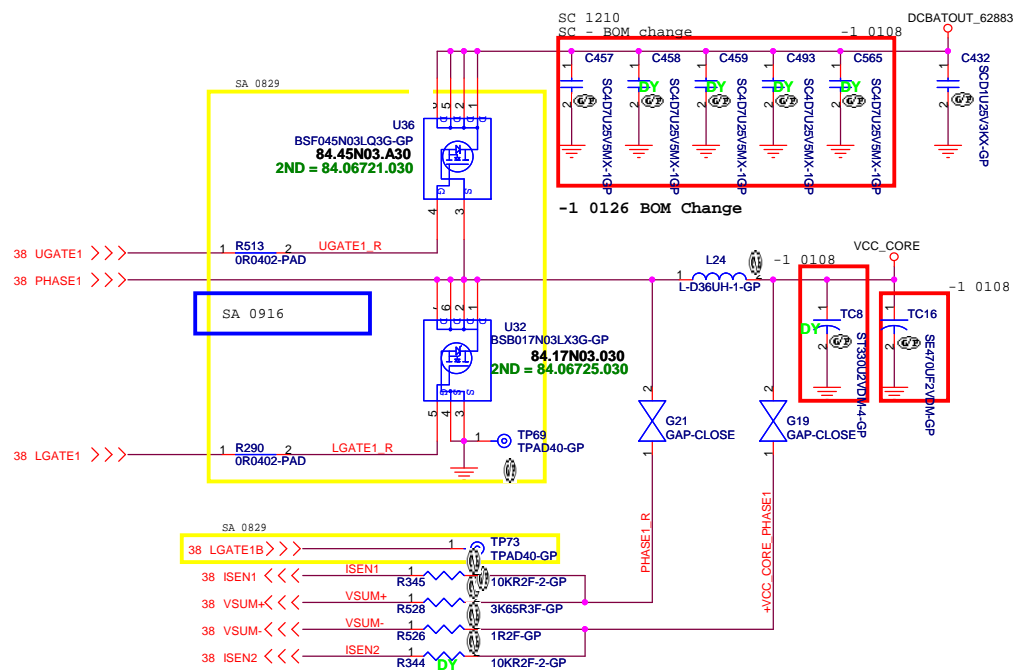
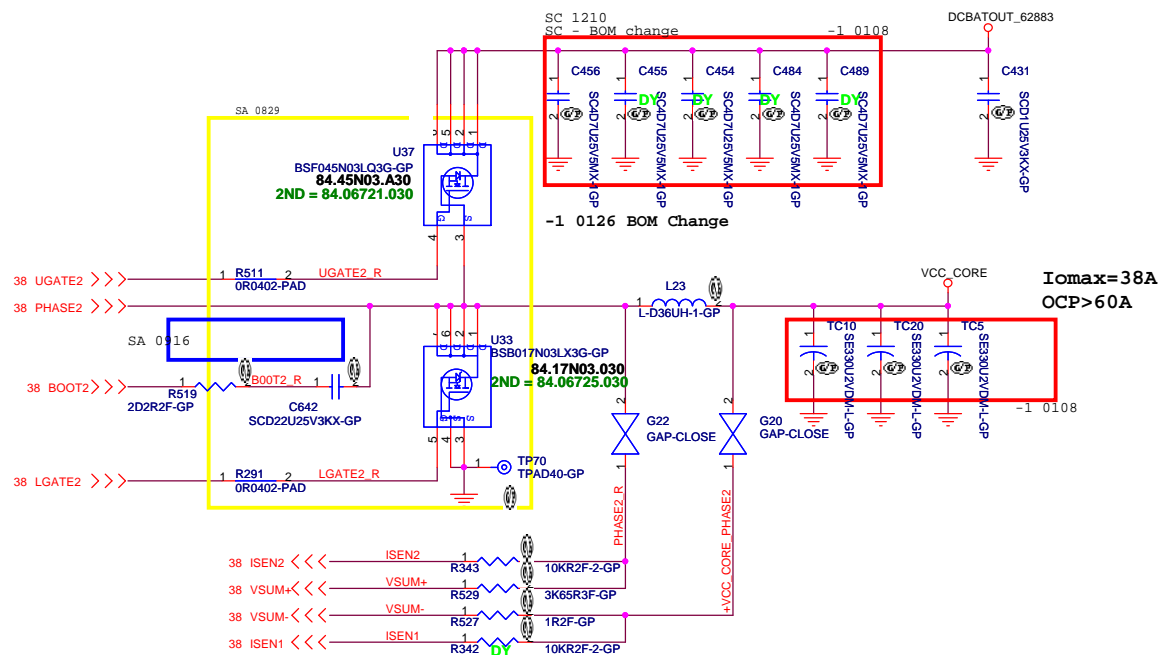


SA 0901



-1 0126 BOM Change -1 0111



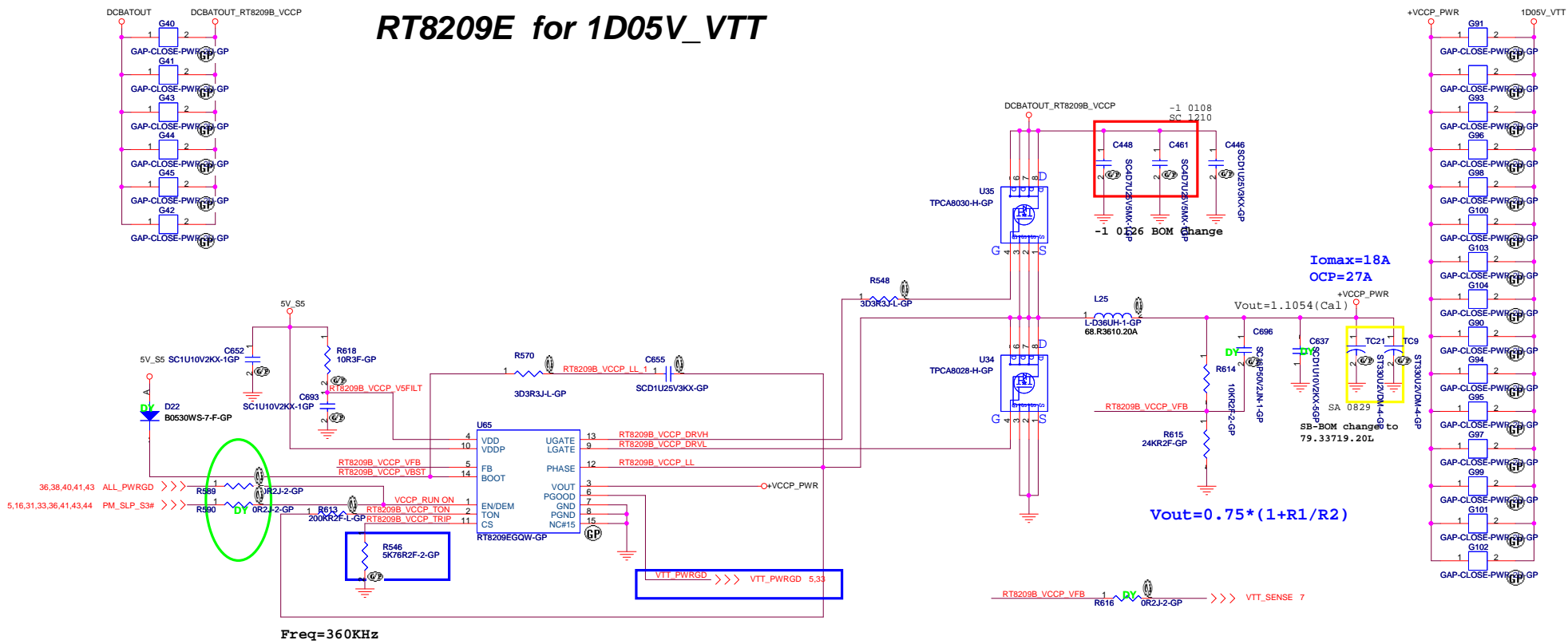




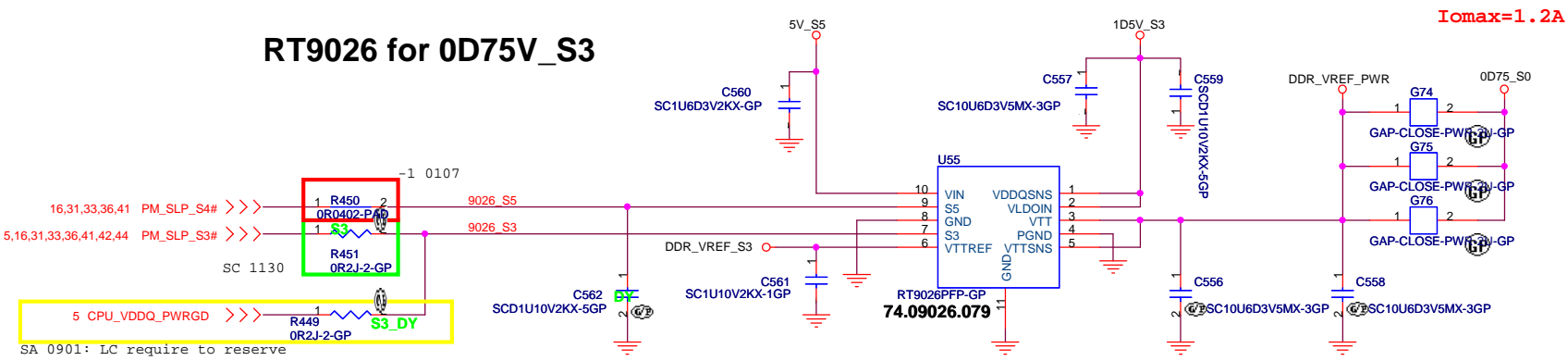
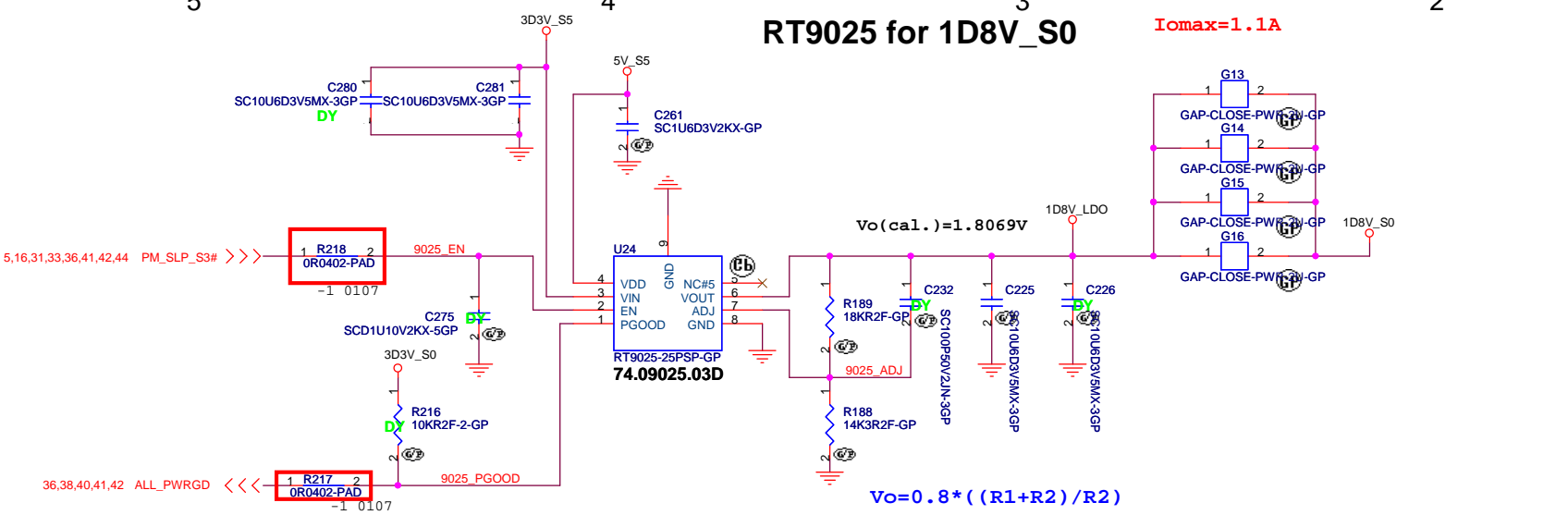




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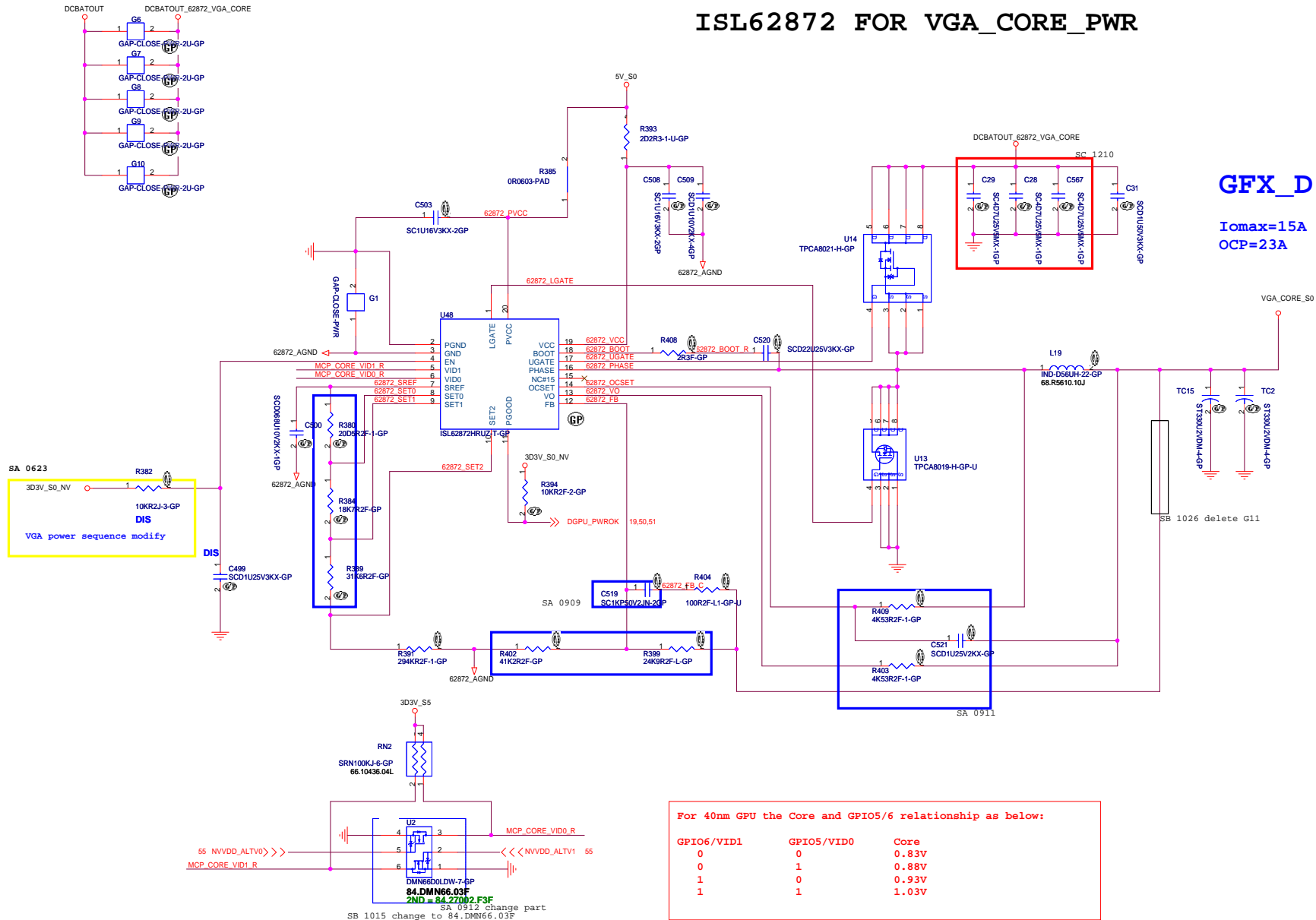


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## ISL62872 FOR VGA\_CORE\_PWR



For 40nm GPU the Core and GPIO5/6 relationship as below:

GPI06/VID1	GPI05/VID0	Cor
0	0	0.8
0	1	0.8
1	0	0.9
1	1	1.0

```
SB 1031 R380 Change to 64.20R55.6DL
R384 Change to 64.18725.6DL
R389 Change to 64.31625.6DL
to rise up VGA voltage for NV suggestion.
```

&lt;Core Design&gt;

緯創資通

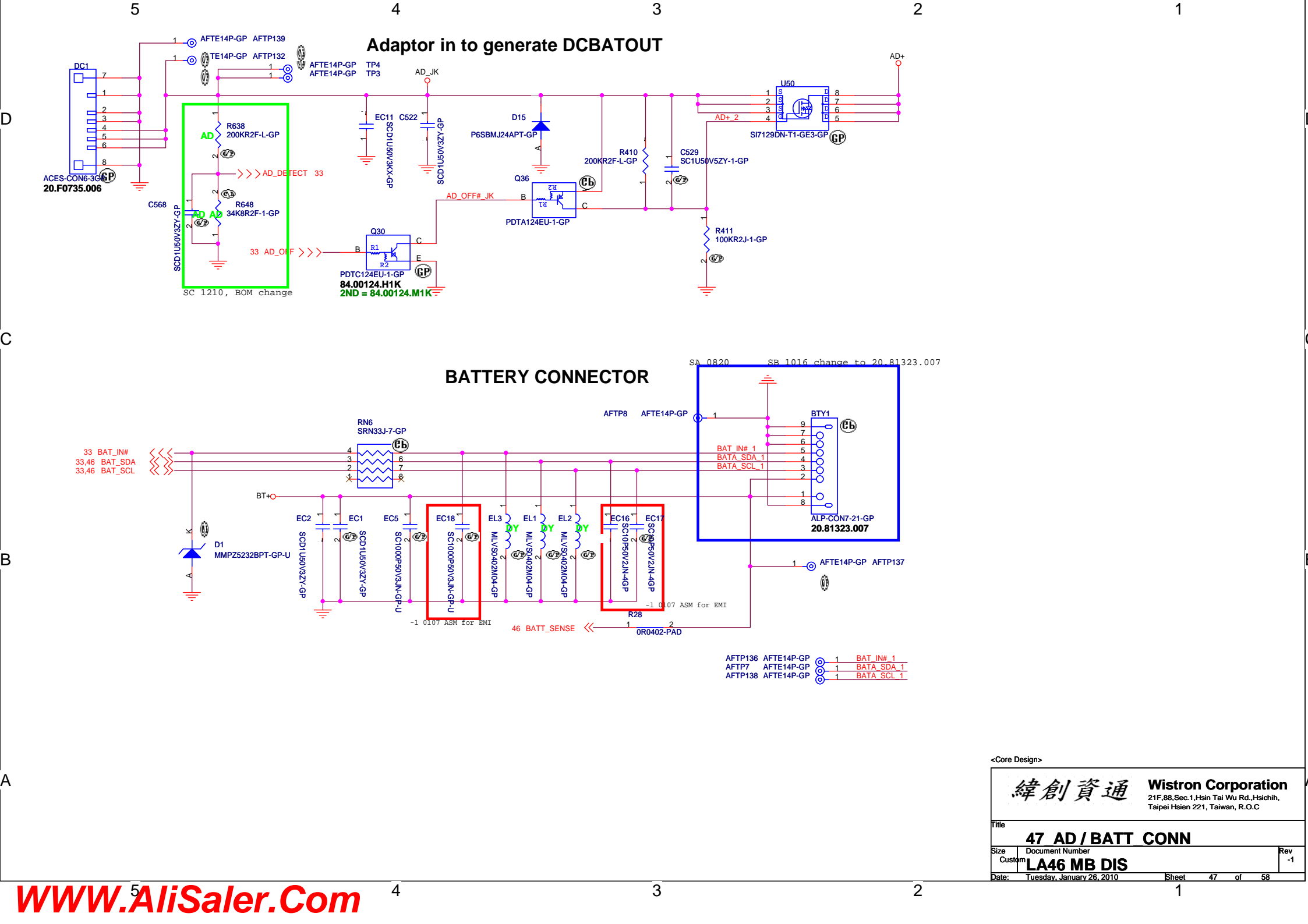
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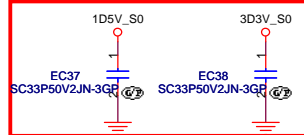
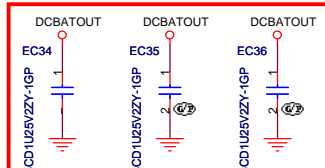
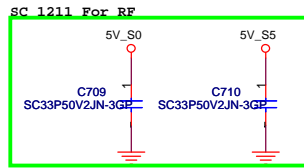
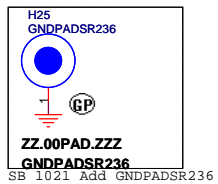
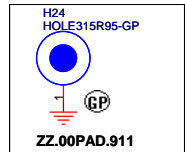
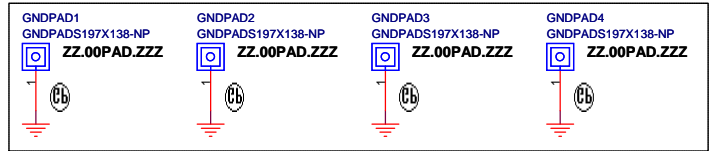
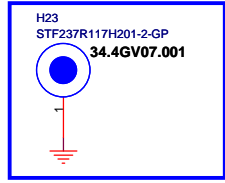
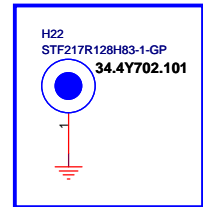
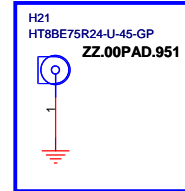
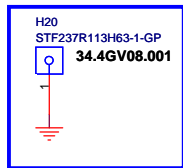
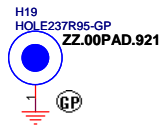
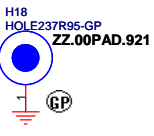
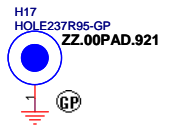
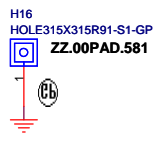
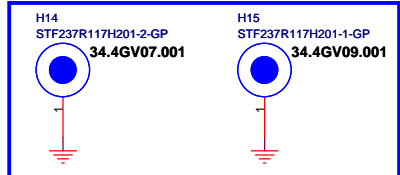
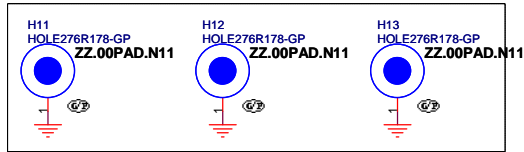
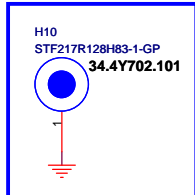
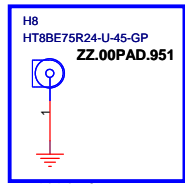
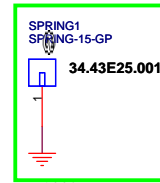
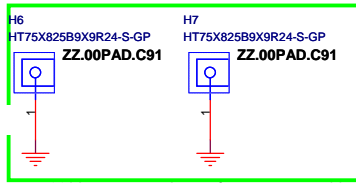
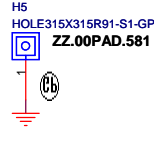
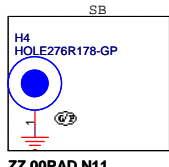
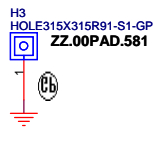
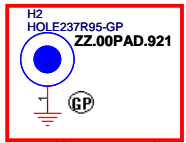
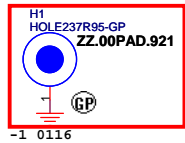
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Custom	<b>LA46 MB DIS</b>

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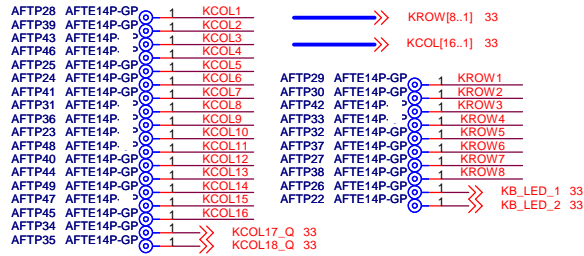
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Taipei Hsien 221, Taiwan, R.O.C

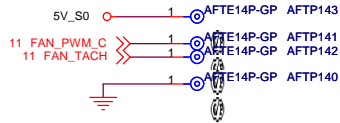
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Size	Document Number	Rev	
A3	LA46 MB DIS	-1	
Date:	Tuesday, January 26, 2010	Sheet	48 of 58



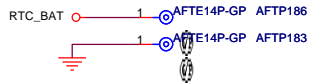
### Near KB1 Keyboard



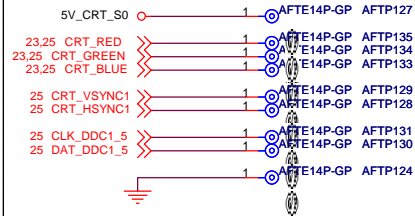
### Near FAN1



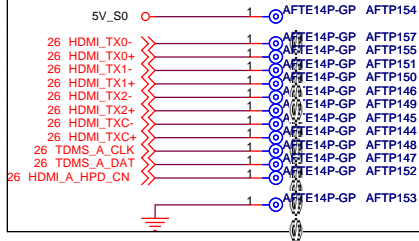
### Near RTC1



### Near CRT\_CN1



### Near HDMI\_CN1



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**49 AFTE TP**

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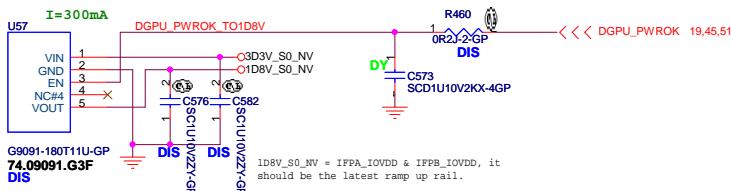
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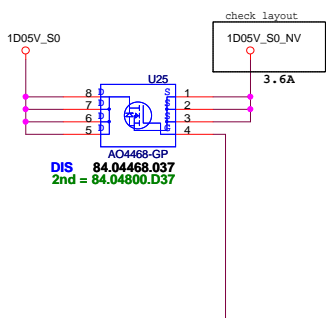
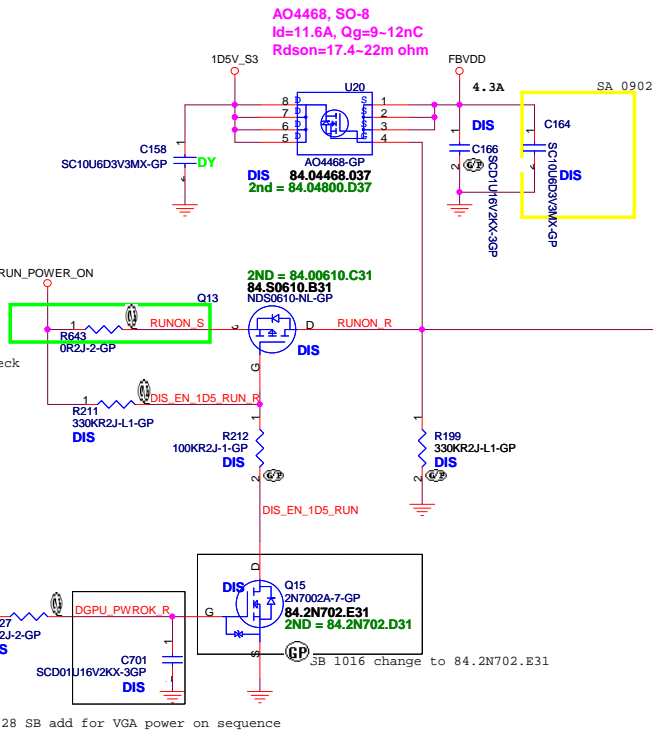
+1.5V to FBVDD Transfer

+1.05V to +1.05V\_NV Transfer

+3VS to 1.8V Transfer

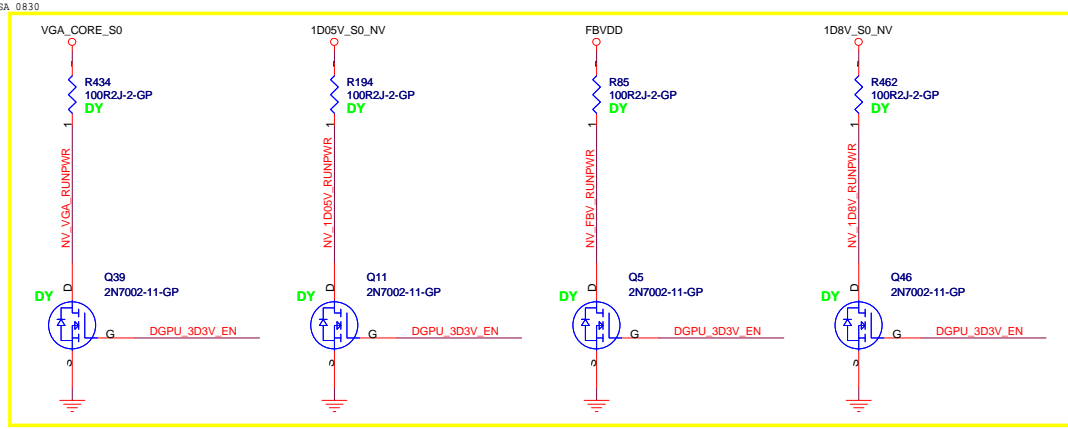
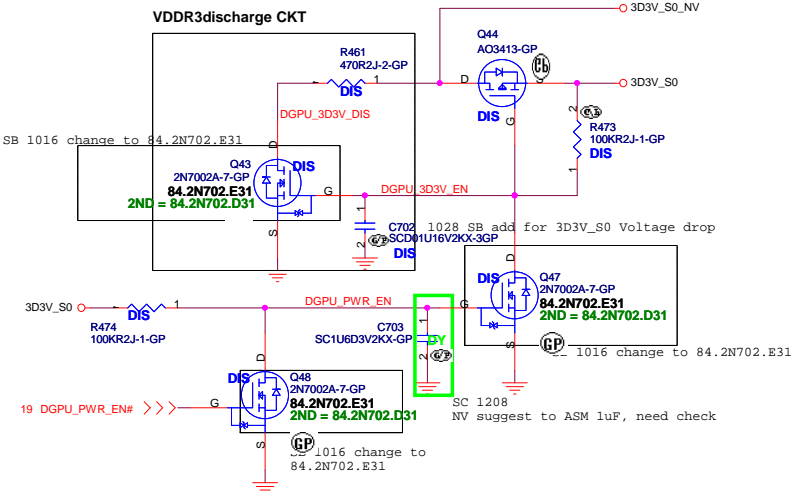


SC 1208  
NV suggest to use 200K, need check



+3VS to 3.3V\_DELAY Transfer

3.3v (580mA)

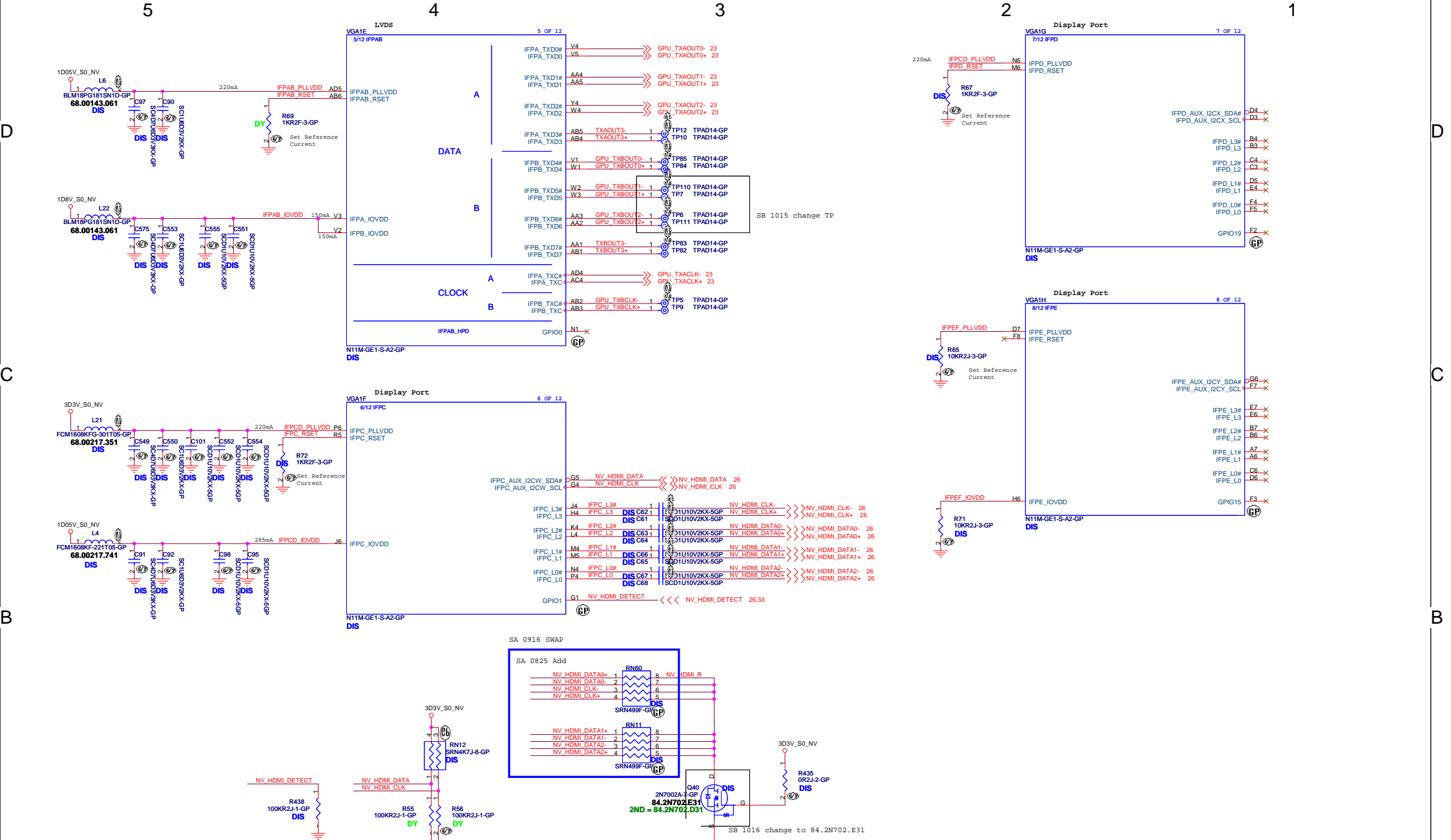


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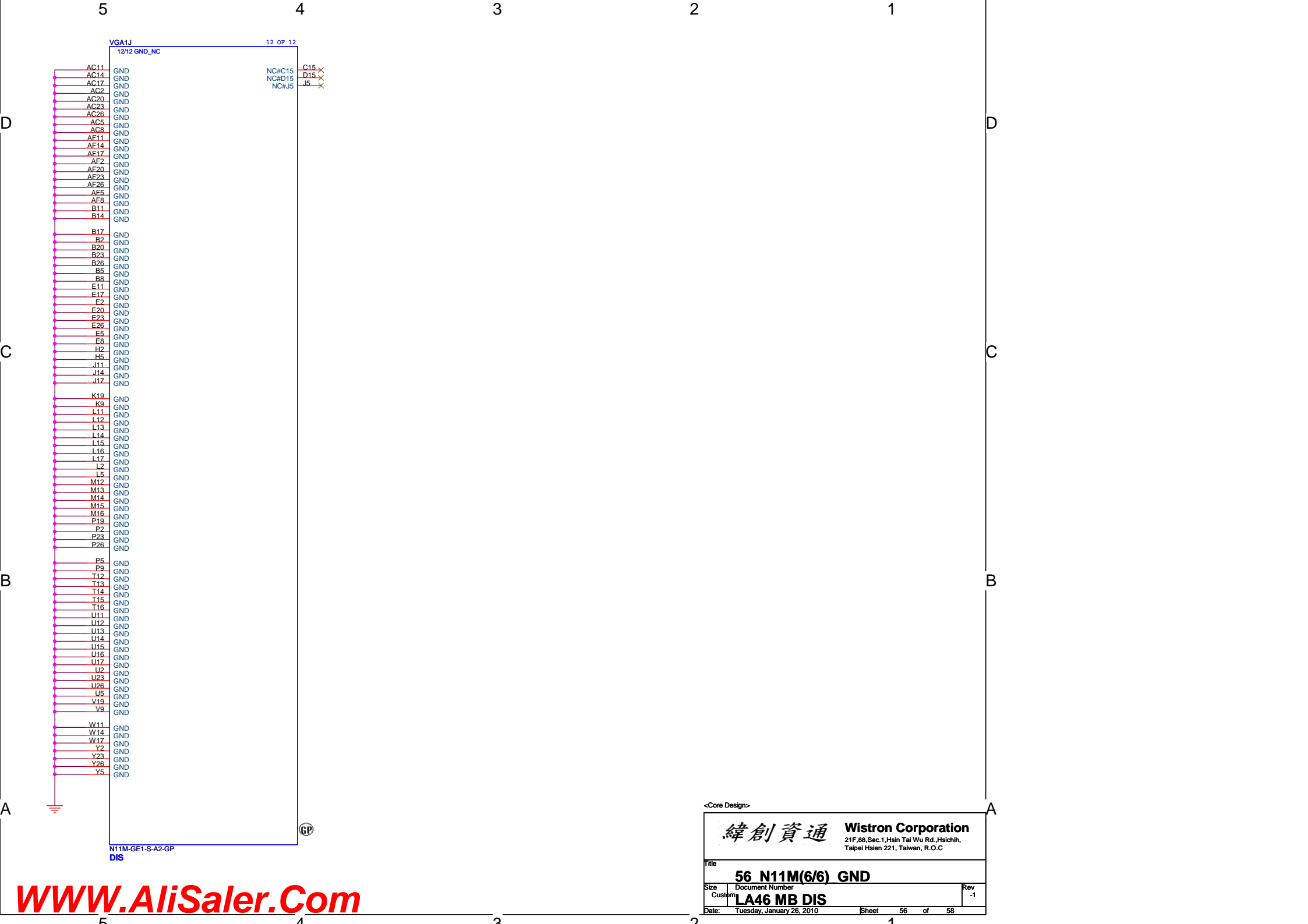




Direct HDMI Connection

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Title			
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12/12 GND\_NC

AC11 GND  
AC14 GND  
AC17 GND  
AC2 GND  
AC20 GND  
AC23 GND  
AC26 GND  
AC5 GND  
AC8 GND  
AE11 GND  
AF14 GND  
AF17 GND  
AF2 GND  
AF20 GND  
AF23 GND  
AF26 GND  
AF5 GND  
AF8 GND  
B11 GND  
B14 GND  
B17 GND  
B2 GND  
B20 GND  
B23 GND  
B26 GND  
B5 GND  
B8 GND  
E11 GND  
E17 GND  
E2 GND  
E20 GND  
E23 GND  
E26 GND  
E5 GND  
E8 GND  
H2 GND  
H5 GND  
J11 GND  
J14 GND  
J17 GND  
K19 GND  
K9 GND  
L11 GND  
L12 GND  
L13 GND  
L14 GND  
L15 GND  
L16 GND  
L17 GND  
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P19 GND  
P2 GND  
P23 GND  
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P5 GND  
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T12 GND  
T13 GND  
T14 GND  
T15 GND  
T16 GND  
U11 GND  
U12 GND  
U13 GND  
U14 GND  
U15 GND  
U16 GND  
U17 GND  
U2 GND  
U23 GND  
U26 GND  
U5 GND  
V19 GND  
V9 GND  
W11 GND  
W14 GND  
W17 GND  
Y2 GND  
Y23 GND  
Y26 GND  
Y5 GND

NC#C15  
NC#D15  
NC#J5

GP

N11M-GE1-S-A2-GP  
DIS

<Core Design>

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